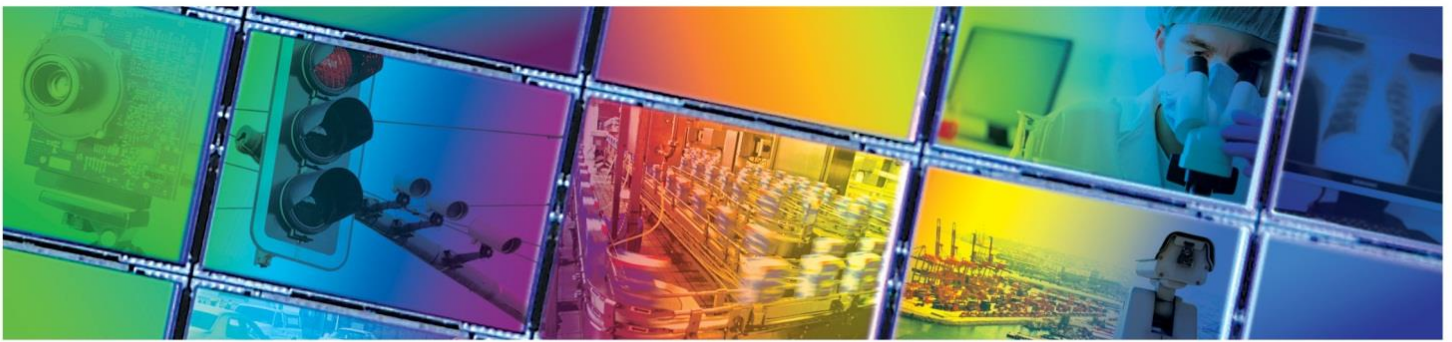


**ON Semiconductor®**



**KAI-02170 IMAGE SENSOR**  
**1920 (H) X 1080 (V) INTERLINE CCD IMAGE SENSOR**



JUNE 11<sup>4</sup>, 2014

**DEVICE PERFORMANCE SPECIFICATION**

**REVISION 1.1 PS-0146**



## TABLE OF CONTENTS

<b>Summary Specification</b> .....	<b>7</b>
Description .....	7
Features .....	7
Applications .....	7
<b>Ordering Information</b> .....	<b>8</b>
KAI-02170 Image Sensor .....	8
Evaluation Support .....	8
<b>Device Description</b> .....	<b>9</b>
Architecture .....	9
Dark Reference Pixels .....	9
Dummy Pixels .....	9
Active Buffer Pixels .....	10
Image Acquisition .....	10
ESD Protection .....	10
Bayer Color Filter Pattern .....	11
TRUESENSE Sparse Color Filter Pattern .....	11
Physical Description .....	12
Pin Description and Device Orientation .....	12
<b>Imaging Performance</b> .....	<b>14</b>
Typical Operation Conditions .....	14
Specifications .....	14
All Configurations .....	14
KAI-02170-ABA and KAI-02170-PBA Configurations .....	15
KAI-02170-CBA and KAI-02170-PBA Configurations .....	15
Linear Signal Range .....	15
<b>Typical Performance Curves</b> .....	<b>16</b>
Quantum Efficiency .....	16
Monochrome with Microlens .....	16
Color (Bayer RGB) with Microlens .....	17
Color (TRUESENSE Sparse CFA) with Microlens .....	17
Angular Quantum Efficiency .....	18
Monochrome with Microlens .....	18
Color (Bayer RGB) with Microlens .....	18
Dark Current versus Temperature .....	19
Power – Estimated .....	20
Power – Estimated – Full Resolution .....	20
Power – Estimated – 1/4 Resolution – 2x2 Binning .....	20
Power – 1/4 Resolution – 2x2 Binning using Variable HCCD XLDR .....	21
Power – 1/4 Resolution – 2x2 Binning using Constant XLDR .....	21
Frame Rates .....	22
Frame Rates – Full Resolution .....	22
Frame Rates – 1/4 Resolution – 2x2 Binning .....	22
Frame Rates – 1/4 Resolution – 2x2 Binning using Variable HCCD XLDR .....	23
Frame Rates – 1/4 Resolution – 2x2 Binning using Constant XLDR .....	23
<b>Defect Definitions</b> .....	<b>24</b>
Operation Conditions for Defect Testing at 40 °C .....	24
Defect Definitions for Testing at 40 °C .....	24
Operation Conditions for Defect Testing at 27 °C .....	25



Defect Definitions for Testing at 27 °C .....	25
Defect Map.....	25
<b>Test Definitions .....</b>	<b>26</b>
OverClocking .....	26
Tests.....	27
Dark Field Global Non-Uniformity.....	27
Global Non-Uniformity.....	27
Global Peak to Peak Non-Uniformity.....	27
Center Non-Uniformity.....	28
Dark Field Defect Test .....	28
Bright Field Defect Test.....	28
<b>Operation.....</b>	<b>29</b>
Absolute Maximum Ratings .....	29
Absolute Maximum Voltage Ratings Between Pins and Ground .....	29
KAI-02150 Compatibility.....	30
Reset Pin, Low Gain (R2ab and R2cd) .....	31
Power Up and Power Down Sequence.....	32
DC Bias Operating Conditions.....	33
AC Operating Conditions.....	34
Clock Levels .....	34
Capacitance.....	35
Device Identification.....	36
Recommended Circuit.....	36
<b>Timing.....</b>	<b>37</b>
Requirements and Characteristics .....	37
Timing Flow Charts.....	38
No Electronic Shutter .....	38
Using the Electronic Shutter.....	39
Timing Tables.....	40
Frame Timing.....	40
Line Timing.....	41
Pixel Timing.....	42
Timing Diagrams .....	43
Frame Timing – Quadrant and Dual VOUTa/VOUTc Readout Modes .....	43
Frame Timing – Single and Dual VOUTa/VOUTb Readout Modes .....	44
Line Timing – Full Resolution – Quadrant and Dual VOUTa/VOUTc Readout Modes .....	45
Line Timing – Full Resolution – Single and Dual VOUTa/VOUTb Readout Modes .....	46
Line Timing – Low Gain, High Gain and XLDR 1/4 Resolution – Quadrant and Dual VOUTa/VOUTc Readout Modes .....	47
Line Timing – Low Gain, High Gain and XLDR 1/4 Resolution – Single and Dual VOUTa/VOUTb Readout Modes .....	48
Electronic Shutter Timing Diagrams .....	49
Pixel Timing – Full Resolution – High Gain Pixel Timing .....	50
Pixel Timing – Full Resolution – Low Gain Pixel Timing .....	51
Pixel Timing – 1/4 Resolution – High Gain Pixel Timing .....	52
Pixel Timing – 1/4 Resolution – Low Gain Pixel Timing.....	53
XLDR Pixel Timing .....	54
Pixel Timing – 1/4 Resolution – XLDR Pixel Timing – Constant HCCD Timing.....	55
Pixel Timing – 1/4 Resolution – XLDR Pixel Timing – Variable HCCD Timing .....	56
VCCD Clock Edge Alignment .....	57
<b>Storage and Handling .....</b>	<b>58</b>
Storage Conditions.....	58
ESD .....	58



---

Cover Glass Care and Cleanliness .....	58
Environmental Exposure .....	58
Soldering Recommendations .....	58
<b>Mechanical Information .....</b>	<b>59</b>
Completed Assembly.....	59
Cover Glass.....	61
Cover Glass Transmission .....	62
<b>Quality Assurance and Reliability.....</b>	<b>63</b>
Quality and Reliability .....	63
Replacement.....	63
Liability of the Supplier .....	63
Liability of the Customer .....	63
Test Data Retention.....	63
Mechanical.....	63
<b>Life Support Applications Policy .....</b>	<b>63</b>
<b>Revision Changes.....</b>	<b>64</b>



## TABLE OF FIGURES

Figure 1: Block Diagram ..... 9

Figure 2: Bayer Color Filter Pattern ..... 11

Figure 3: Sparse Color Filter Pattern ..... 11

Figure 4: Package Pin Designations - Top View..... 12

Figure 5: High Gain Linear Signal Range..... 15

Figure 6: Low Gain Linear Signal Range ..... 15

Figure 7: Monochrome with Microlens Quantum Efficiency..... 16

Figure 8: Color (Bayer RGB) with Microlens Quantum Efficiency ..... 17

Figure 9: Color (TRUESENSE Sparse CFA) with Microlens Quantum Efficiency ..... 17

Figure 10: Monochrome with Microlens Angular Quantum Efficiency ..... 18

Figure 11: Color (Bayer RGB) with Microlens Angular Quantum Efficiency ..... 18

Figure 12: Dark Current versus Temperature ..... 19

Figure 13: Power – Full Resolution ..... 20

Figure 14: Power – 1/4 Resolution – Constant HCCD ..... 20

Figure 15: Power – 1/4 Resolution – Variable HCCD XLDR ..... 21

Figure 16: Power – 1/4 Resolution - Constant HCCD XLDR..... 21

Figure 17: Frame Rates – Full Resolution ..... 22

Figure 18: Frame Rates – 1/4 Resolution – Constant HCCD..... 22

Figure 19: Frame Rates – 1/4 Resolution - Variable HCCD ..... 23

Figure 20: Frame Rates – 1/4 Resolution - Constant HCCD XLDR ..... 23

Figure 21: Regions of Interest ..... 26

Figure 22: Equivalent Circuit for Reset Gate, low Gain (R2ab and R2cd) ..... 31

Figure 23: Power Up and Power Down Sequence ..... 32

Figure 24: Output Amplifier ..... 33

Figure 25: Device Identification Recommended Circuit ..... 36

Figure 26: Timing Flow When Electronic Shutter is Not Used ..... 38

Figure 27: Timing Flow Chart Using the Electronic Shutter for Exposure Control..... 39

Figure 28: Frame Timing Diagram Quadrant and Dual VOUTa/VOUTc Readout Modes ..... 43

Figure 29: Frame Timing Diagram Single and Dual VOUTa/VOUTb Readout Modes ..... 44

Figure 30: Line Timing Diagram – Full Resolution – Quadrant and Dual VOUTa/VOUTc Modes..... 45

Figure 31: Line Timing Diagram – Full Resolution – Single and Dual VOUTa/VOUTb Modes ..... 46

Figure 32: Line Timing Diagram – 1/4 Resolution – Quadrant and Dual VOUTa/VOUTc Modes ..... 47

Figure 33: Line Timing Diagram – 1/4 Resolution – Single and Dual VOUTa/VOUTb Modes..... 48

Figure 34: Electronic Shutter Timing ..... 49

Figure 35: Frame/Electronic Shutter Timing..... 49

Figure 36: Pixel Timing Diagram – Full Resolution – High Gain ..... 50

Figure 37: Pixel Timing Diagram – Full Resolution – Low Gain..... 51

Figure 38: Pixel Timing Diagram – 1/4 Resolution – High Gain..... 52

Figure 39: Pixel Timing Diagram – 1/4 Resolution – Low Gain ..... 53

Figure 40: XLDR Timing - AFE Connections Block Diagram..... 54

Figure 41: Pixel Timing Diagram – 1/4 Resolution – XLDR – Constant HCCD Timing ..... 55

Figure 42: Pixel Timing Diagram – 1/4 Resolution – XLDR – Variable HCCD Timing..... 56

Figure 43: VCCD Clock Rise Time, Fall Time, and Edge Alignment..... 57

Figure 44: Completed Assembly (1 of 2)..... 59

Figure 45: Completed Assembly (2 of 2) ..... 60

Figure 46: Cover Glass ..... 61

Figure 47: Cover Glass Transmission..... 62



## TABLE OF TABLES

Table 1: Values for NH and NV When Operating the Sensor in the Various Modes of Resolution .....	38
Table 2: Frame Timing .....	40
Table 3: Line Timing .....	41
Table 4: Pixel Timing .....	42



## Summary Specification

### KAI-02170 Image Sensor

#### DESCRIPTION

The KAI-02170 Image Sensor is a 2-megapixel CCD in a 1 inch optical format. Based on the TRUESENSE 7.4 micron Interline Transfer CCD Platform, the sensor provides very high smear rejection and up to 82 dB linear dynamic range through the use of a unique dual-gain amplifier. A flexible readout architecture enables use of 1, 2, or 4 outputs for full resolution readout up to 60 frames per second, while a vertical overflow drain structure suppresses image blooming and enables electronic shuttering for precise exposure control.

The sensor is available with the TRUESENSE Sparse Color Filter Pattern, a technology which provides a 2x improvement in light sensitivity compared to a standard color Bayer part.

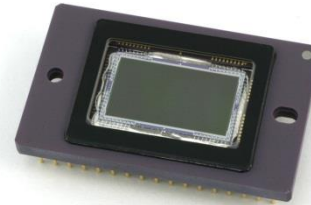
The sensor shares common pin-out and electrical configurations with a full family of Truesense Imaging Interline Transfer CCD image sensors, allowing a single camera design to be leveraged in support of multiple devices.

#### FEATURES

- Superior smear rejection
- Up to 82 dB linear dynamic range
- Bayer Color Pattern, TRUESENSE Sparse Color Filter Pattern, and Monochrome configurations
- Progressive scan & flexible readout architecture
- High frame rate
- High sensitivity - Low noise architecture
- Package pin reserved for device identification

#### APPLICATIONS

- Industrial Imaging and Inspection
- Traffic
- Surveillance



Parameter	Typical Value
Architecture	Interline CCD; Progressive Scan
Total Number of Pixels	1984 (H) x 1124 (V)
Number of Effective Pixels	1936 (H) x 1096 (V)
Number of Active Pixels	1920 (H) x 1080 (V)
Pixel Size	7.4 $\mu\text{m}$ (H) x 7.4 $\mu\text{m}$ (V)
Active Image Size	14.2 mm (H) x 8.0 mm (V) 16.3 mm (diag) 1 inch format
Aspect Ratio	16:9
Number of Outputs	1, 2, or 4
Charge Capacity	44,000 electrons
Output Sensitivity	8.7 $\mu\text{V}/\text{e}^-$ (low), 33 $\mu\text{V}/\text{e}^-$ (high)
Quantum Efficiency R, G, B (-CXA, -PXA) Pan (-AXA, -PXA)	38%, 42%, 43% 52%
Read Noise (F = 40 MHz)	12 electrons rms
Dark Current Photodiode VCCD	3 electrons/s 145 electrons/s
Dark Current Doubling Temp Photodiode VCCD	7 $^{\circ}\text{C}$ 9 $^{\circ}\text{C}$
Dynamic Range High gain amp (40 MHz) Dual amp, 2x2 bin (40 MHz)	70 dB 82 dB
Charge Transfer Efficiency	0.999999
Blooming Suppression	> 1000 X
Smear	-115 dB
Image Lag	< 10 electrons
Maximum Pixel Clock Speed	40 MHz
Maximum Frame Rates Quad Output Dual Output Single Output	60 fps 30 fps 15 fps
Package	68 pin PGA
Cover Glass	AR Coated, 2 Sides

All parameters are specified at T = 40  $^{\circ}\text{C}$  unless otherwise noted.



## Ordering Information

### KAI-02170 IMAGE SENSOR

Catalog Number	Product Name	Description	Marking Code
4H2248	KAI-02170-ABA-JD-BA	Monochrome, Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-02170-ABA Serial Number
4H2249 <sup>(2)</sup>	KAI-02170-ABA-JD-AE	Monochrome, Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	
4H2251	KAI-02170-CBA-JD-BA	Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-02170-CBA Serial Number
4H2252 <sup>(2)</sup>	KAI-02170-CBA-JD-AE	Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	
4H2254	KAI-02170-PBA-JD-BA	Color (TRUESENSE Sparse CFA), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-02170-PBA Serial Number
4H2255 <sup>(2)</sup>	KAI-02170-PBA-JD-AE	Color (TRUESENSE Sparse CFA), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR coating (both sides), Engineering Grade	

## EVALUATION SUPPORT

<u>Catalog Number</u>	<u>Product Name</u>	<u>Description</u>
<a href="#">4H2207</a>	<a href="#">KEM-4H2207-G2 FPGA Board-14-40</a>	<a href="#">FPGA Board for IT-CCD Evaluation Hardware</a>
<a href="#">4H2208</a>	<a href="#">KEH-4H2208-KAI-68 Pin Imager Board</a>	<a href="#">68 Pin Imager Board for IT-CCD Evaluation Hardware</a>
<a href="#">4H2211</a>	<a href="#">KEL-4H2211-Lens Mount Kit</a>	<a href="#">Lens Mount Kit for IT-CCD Evaluation Hardware</a>
<a href="#">4H2269</a>	<a href="#">KEH-4H2269-KAI-68 Pin Narrow Probe Card</a>	<a href="#">68 Pin Probe Card (narrow socket)</a>
<a href="#">4H2268</a>	<a href="#">KEH-4H2268-KAI-68 Pin Wide Probe Card</a>	<a href="#">68 Pin Probe Card (wide socket)</a>

1. ~~Engineering Grade part numbers are listed for informational purposes only. Engineering Grade part numbers are not available for orders at this time. Please contact Truesense Imaging for availability dates~~

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at [www.truesenseimaging.com](http://www.truesenseimaging.com).

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.  
1964 Lake Avenue  
Rochester, New York 14615

Phone: (585) 784-5500  
E-mail: [info@truesenseimaging.com](mailto:info@truesenseimaging.com)

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.





## Device Description

### ARCHITECTURE

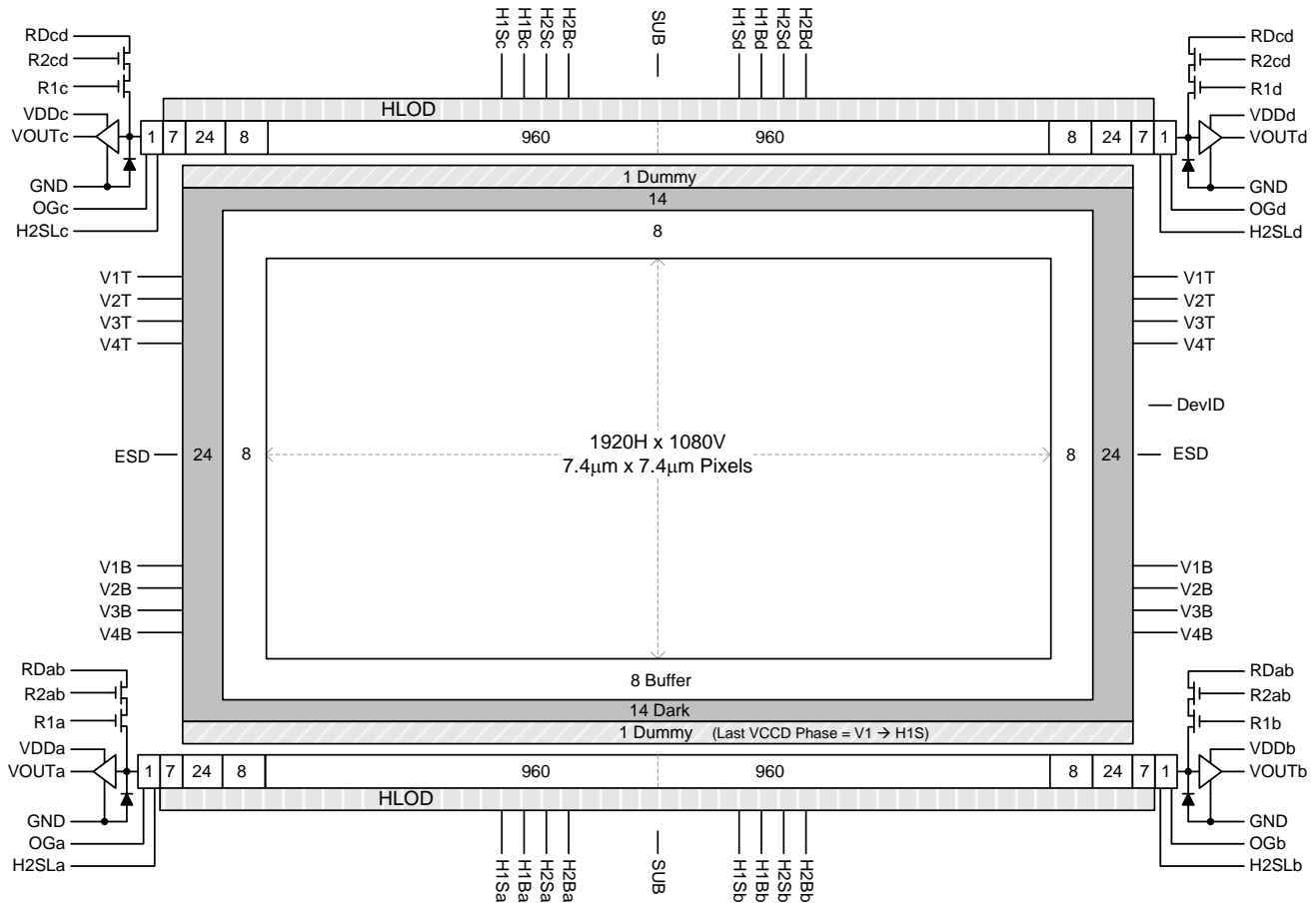


Figure 1: Block Diagram

### DARK REFERENCE PIXELS

There are 14 dark reference rows at the top and 14 dark rows at the bottom of the image sensor. The 24 dark columns on the left or right side of the image sensor should be used as a dark reference.

Under normal circumstances use only the center 22 columns of the 24 column dark reference due to potential light leakage.

### DUMMY PIXELS

Within each horizontal shift register there are 8 leading additional shift phases. These pixels are designated as dummy pixels and should not be used to determine a dark reference level.

In addition, there is one dummy row of pixels at the top and bottom of the image.



## ACTIVE BUFFER PIXELS

8 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels. These pixels are light sensitive but are not tested for defects and non-uniformities.

## IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming

## ESD PROTECTION

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor. See Power Up and Power Down Sequence section.





## PHYSICAL DESCRIPTION

### Pin Description and Device Orientation

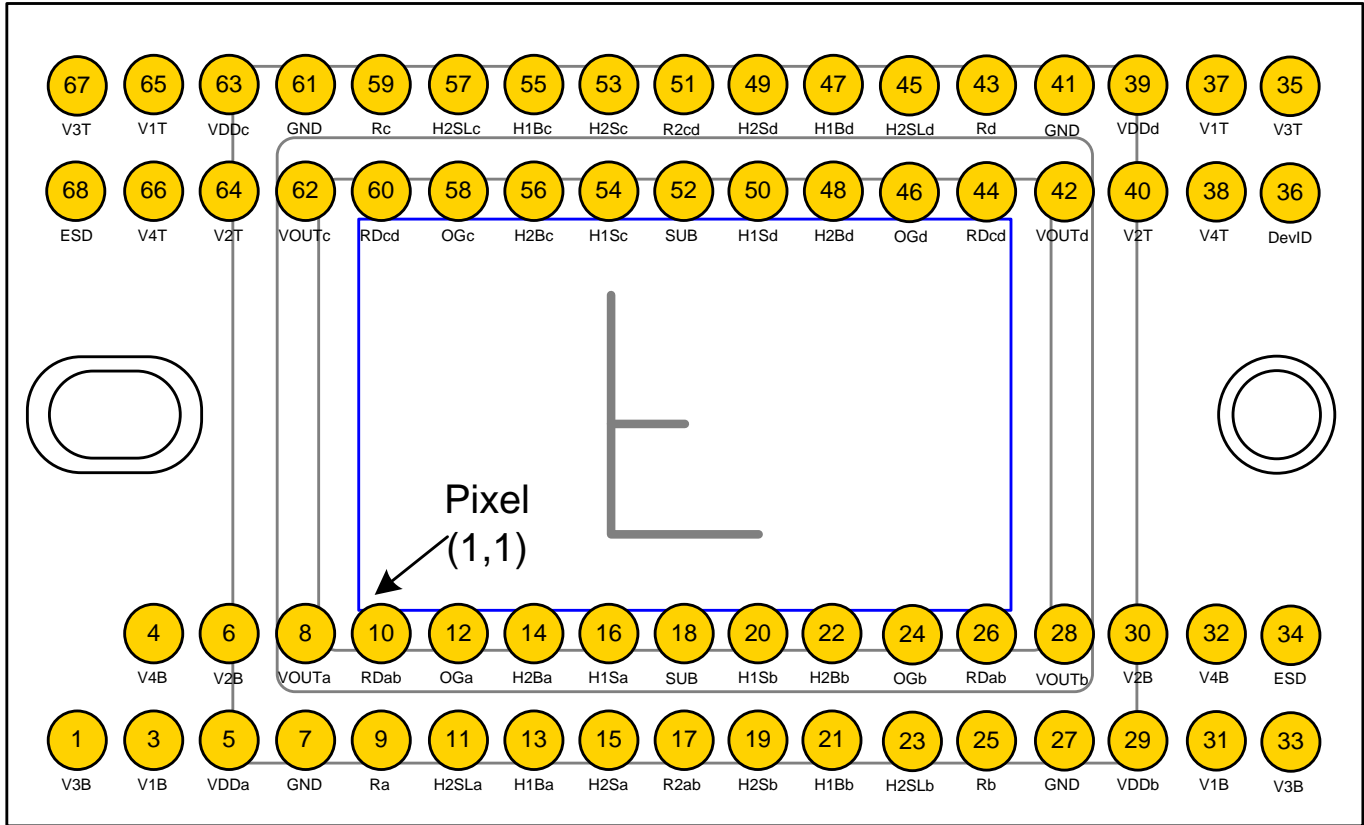


Figure 4: Package Pin Designations - Top View



Pin	Name	Description
1	V3B	Vertical CCD Clock, Phase 3, Bottom
3	V1B	Vertical CCD Clock, Phase 1, Bottom
4	V4B	Vertical CCD Clock, Phase 4, Bottom
5	VDDa	Output Amplifier Supply, Quadrant a
6	V2B	Vertical CCD Clock, Phase 2, Bottom
7	GND	Ground
8	VOUTa	Video Output, Quadrant a
9	Ra	Reset Gate, Standard (high) Gain, Quadrant a
10	RDab	Reset Drain, Quadrants a and b
11	H2SLa	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a
12	OGa	Output Gate, Quadrant a
13	H1Ba	Horizontal CCD Clock, Phase 1, Barrier, Quadrant a
14	H2Ba	Horizontal CCD Clock, Phase 2, Barrier, Quadrant a
15	H2Sa	Horizontal CCD Clock, Phase 2, Storage, Quadrant a
16	H1Sa	Horizontal CCD Clock, Phase 1, Storage, Quadrant a
17	R2ab	Reset Gate, Low Gain, Quadrants a and b
18	SUB	Substrate
19	H2Sb	Horizontal CCD Clock, Phase 2, Storage, Quadrant b
20	H1Sb	Horizontal CCD Clock, Phase 1, Storage, Quadrant b
21	H1Bb	Horizontal CCD Clock, Phase 1, Barrier, Quadrant b
22	H2Bb	Horizontal CCD Clock, Phase 2, Barrier, Quadrant b
23	H2SLb	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant b
24	OGb	Output Gate, Quadrant b
25	Rb	Reset Gate, Standard (high) Gain, Quadrant b
26	RDab	Reset Drain, Quadrants a and b
27	GND	Ground
28	VOUTb	Video Output, Quadrant b
29	VDDb	Output Amplifier Supply, Quadrant b
30	V2B	Vertical CCD Clock, Phase 2, Bottom
31	V1B	Vertical CCD Clock, Phase 1, Bottom
32	V4B	Vertical CCD Clock, Phase 4, Bottom
33	V3B	Vertical CCD Clock, Phase 3, Bottom
34	ESD	ESD Protection Disable

Pin	Name	Description
68	ESD	ESD Protection Disable
67	V3T	Vertical CCD Clock, Phase 3, Top
66	V4T	Vertical CCD Clock, Phase 4, Top
65	V1T	Vertical CCD Clock, Phase 1, Top
64	V2T	Vertical CCD Clock, Phase 2, Top
63	VDDc	Output Amplifier Supply, Quadrant c
62	VOUTc	Video Output, Quadrant c
61	GND	Ground
60	RDcd	Reset Drain, Quadrants c and d
59	Rc	Reset Gate, Standard (high) Gain, Quadrant c
58	OGc	Output Gate, Quadrant c
57	H2SLc	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c
56	H2Bc	Horizontal CCD Clock, Phase 2, Barrier, Quadrant c
55	H1Bc	Horizontal CCD Clock, Phase 1, Barrier, Quadrant c
54	H1Sc	Horizontal CCD Clock, Phase 1, Storage, Quadrant c
53	H2Sc	Horizontal CCD Clock, Phase 2, Storage, Quadrant c
52	SUB	Substrate
51	R2cd	Reset Gate, Low Gain, Quadrants c and d
50	H1Sd	Horizontal CCD Clock, Phase 1, Storage, Quadrant d
49	H2Sd	Horizontal CCD Clock, Phase 2, Storage, Quadrant d
48	H2Bd	Horizontal CCD Clock, Phase 2, Barrier, Quadrant d
47	H1Bd	Horizontal CCD Clock, Phase 1, Barrier, Quadrant d
46	OGd	Output Gate, Quadrant b
45	H2SLd	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d
44	RDcd	Reset Drain, Quadrants c and d
43	Rd	Reset Gate, Standard (high) Gain, Quadrant d
42	VOUTd	Video Output, Quadrant d
41	GND	Ground
40	V2T	Vertical CCD Clock, Phase 2, Top
39	VDDd	Output Amplifier Supply, Quadrant d
38	V4T	Vertical CCD Clock, Phase 4, Top
37	V1T	Vertical CCD Clock, Phase 1, Top
36	DevID	Device Identification
35	V3T	Vertical CCD Clock, Phase 3, Top

Notes:

1. Liked named pins are internally connected and should have a common drive signal.



## Imaging Performance

### TYPICAL OPERATION CONDITIONS

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.

Description	Condition	Notes
Light Source	Continuous red, green and blue LED illumination	1
Operation	Nominal operating voltages and timing	

Notes:

- For monochrome sensor, only green LED used.

### SPECIFICATIONS

#### All Configurations

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes
Dark Field Global Non-Uniformity	DSNU	-	-	2.0	mVpp	Die	27, 40	
Bright Field Global Non-Uniformity		-	2.0	5.0	%rms	Die	27, 40	1
Bright Field Global Peak to Peak Non-Uniformity	PRNU	-	5.0	15.0	%pp	Die	27, 40	1
Bright Field Center Non-Uniformity		-	1.0	2.0	%rms	Die	27, 40	1
Maximum Photo-response Nonlinearity High Gain (4,000 to 20,000 electrons) High Gain (4,000 to 40,000 electrons) Low Gain (8,000 to 80,000 electrons)	NL_HG1 NL_HG2 NL_LG1	- - -	2 3 6	- - -	% % %	Design		
Maximum Gain Difference Between Outputs	$\Delta G$	-	-	10	%	Design		2
Horizontal CCD Charge Capacity	HNe	-	90	-	ke <sup>-</sup>	Design		
Vertical CCD Charge Capacity	VNe	-	60	-	ke <sup>-</sup>	Design		
Photodiode Charge Capacity	PNe	-	44	-	ke <sup>-</sup>	Die	27, 40	3
Floating Diffusion Capacity – High Gain	FNe_HG	40	-	-	ke <sup>-</sup>	Die	27, 40	
Floating Diffusion Capacity – Low Gain	FNe_LG	160	-	-	ke <sup>-</sup>	Die	27, 40	
Horizontal CCD Charge Transfer Efficiency	HCTE	0.999995	0.999999	-		Die		
Vertical CCD Charge Transfer Efficiency	VCTE	0.999995	0.999999	-		Die		
Photodiode Dark Current	I <sub>pd</sub>	-	7	70	e/p/s	Die	40	
Vertical CCD Dark Current	I <sub>vd</sub>	-	140	400	e/p/s	Die	40	
Image Lag	Lag	-	-	10	e <sup>-</sup>	Design		
Antiblooming Factor	Xab	1000	-	-		Design		
Vertical Smear	Smr	-	-115	-	dB	Design		
Read Noise	$n_{e-T}$	-	12 45	-	e <sup>-</sup> rms	Design	High gain Low gain	4
Dynamic Range, Standard	DR	-	70.5	-	dB	Design		4, 5
Dynamic Range, extended linear dynamic range mode (XLDR)	XLDR	-	82.5	-	dB	Design		4, 5
Output Amplifier DC Offset	V <sub>odc</sub>	-	9.0	-	V	Die	27, 40	
Output Amplifier Bandwidth	f <sub>-3db</sub>	-	250	-	MHz	Die		6
Output Amplifier Impedance	ROUT	-	127	-	Ohms	Die	27, 40	
Output Amplifier Sensitivity High Gain Low Gain	$\Delta V/\Delta N$	- -	33 8.7	- -	$\mu V/e^-$	Design		



### KAI-02170-ABA and KAI-02170-PBA Configurations

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes
Peak Quantum Efficiency	QE <sub>max</sub>	-	52	-	%	Design		
Peak Quantum Efficiency Wavelength	λQE	-	500	-	nm	Design		

### KAI-02170-CBA and KAI-02170-PBA Configurations

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Notes
Peak Quantum Efficiency	QE <sub>max</sub>	-	43	-	%	Design		
Blue			42					
Green			38					
Peak Quantum Efficiency Wavelength	λQE	-	470	-	nm	Design		
Blue			540					
Green			620					
Red								

Notes:

1. Per color
2. Value is over the range of 10% to 100% of linear signal level saturation.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is 440 mV. This value is determined while operating the device in the low gain mode. VAB value assigned is valid for both modes; high gain or low gain.
4. At 40 MHz.
5. Uses 20LOG(PNe/n<sub>e-T</sub>)
6. Assumes 5pF load

### Linear Signal Range

#### High Gain

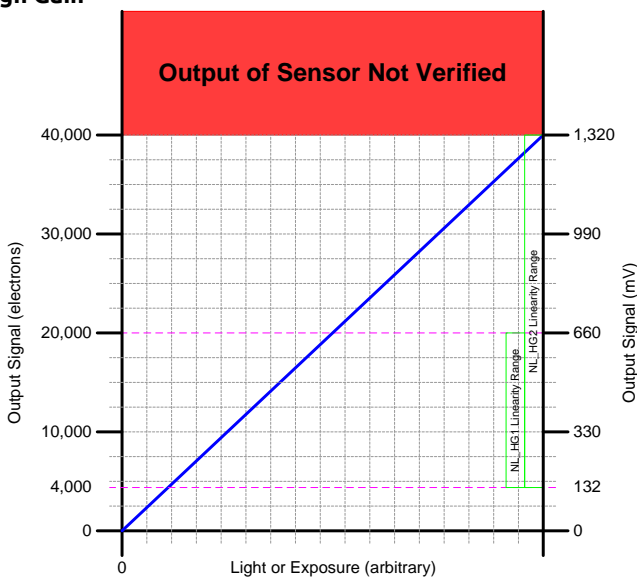


Figure 5: High Gain Linear Signal Range

#### Low Gain

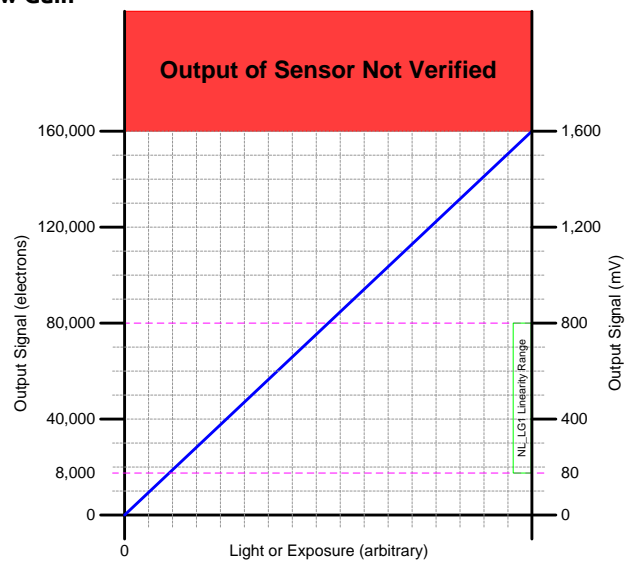


Figure 6: Low Gain Linear Signal Range



## Typical Performance Curves

### QUANTUM EFFICIENCY

#### Monochrome with Microlens

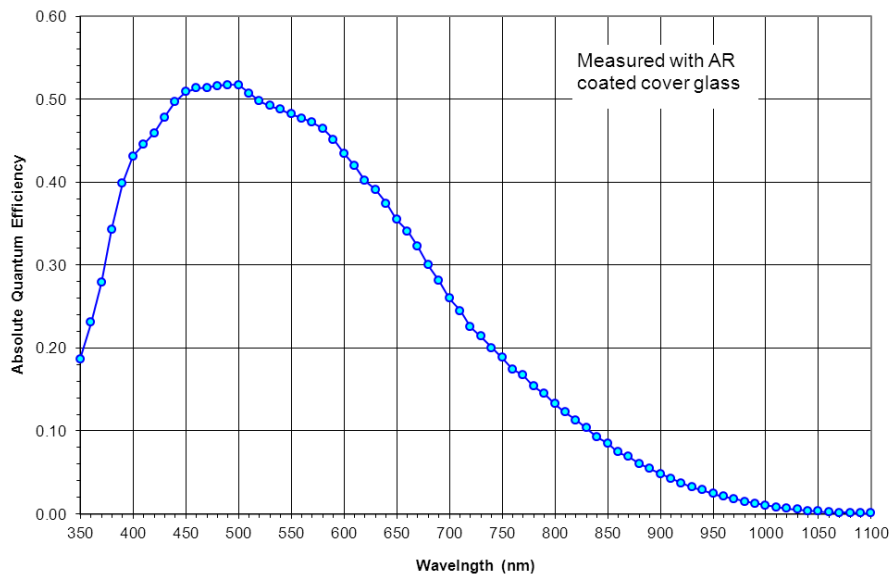


Figure 7: Monochrome with Microlens Quantum Efficiency





### Color (Bayer RGB) with Microlens

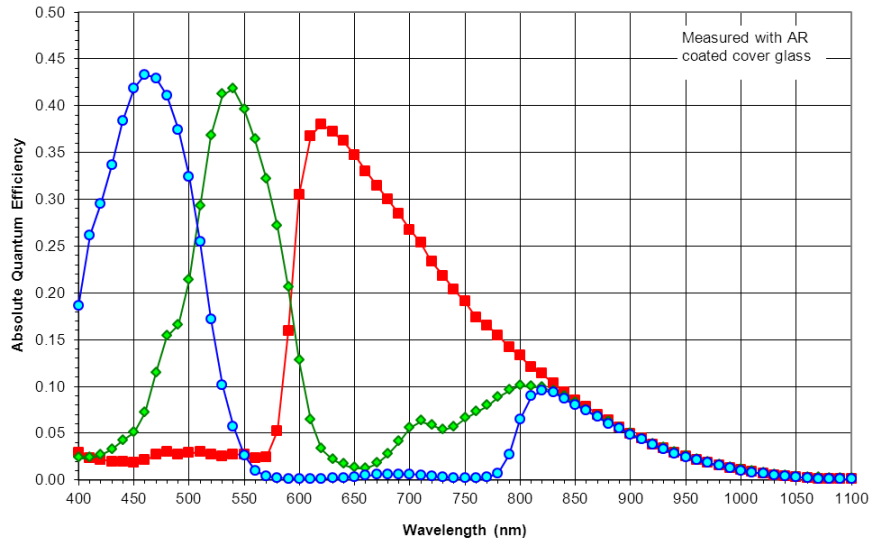


Figure 8: Color (Bayer RGB) with Microlens Quantum Efficiency

### Color (TRUESENSE Sparse CFA) with Microlens

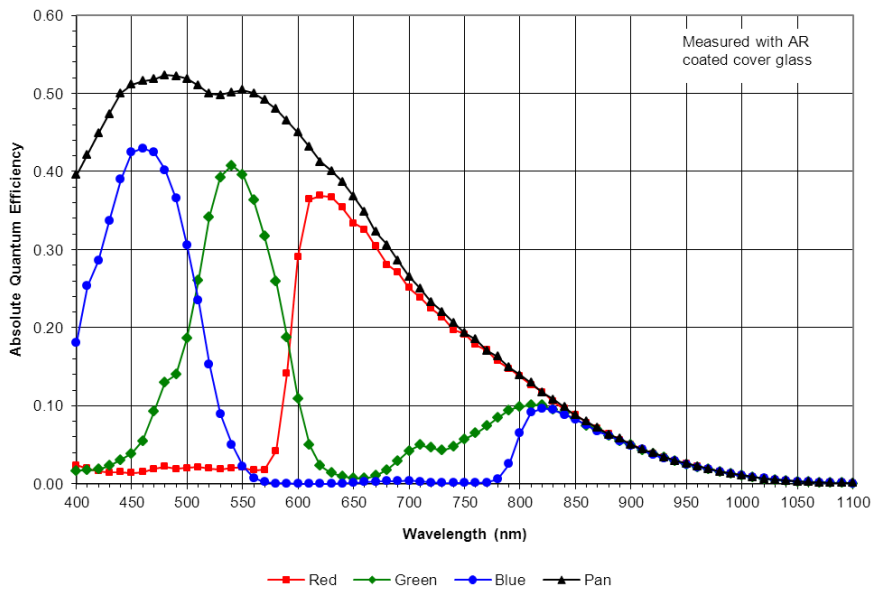


Figure 9: Color (TRUESENSE Sparse CFA) with Microlens Quantum Efficiency



### ANGULAR QUANTUM EFFICIENCY

For the curves marked "Horizontal", the incident light angle is varied in a plane parallel to the HCCD.

For the curves marked "Vertical", the incident light angle is varied in a plane parallel to the VCCD.

### Monochrome with Microlens

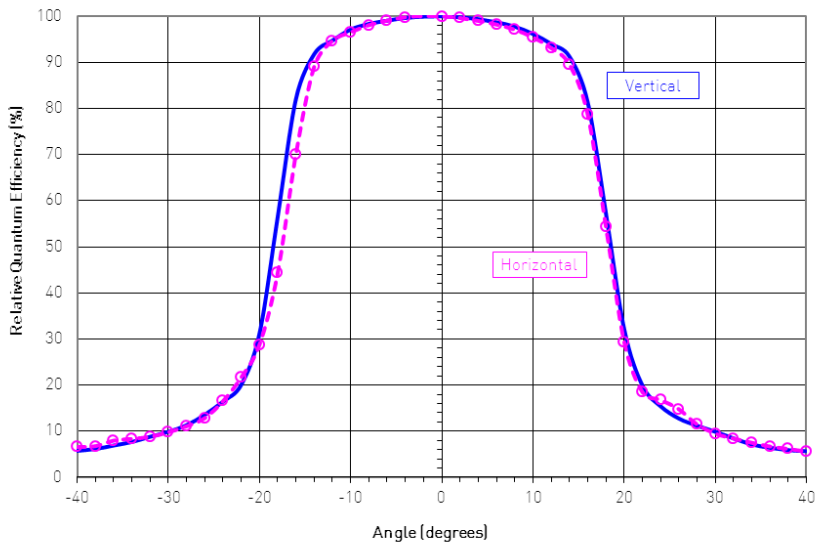


Figure 10: Monochrome with Microlens Angular Quantum Efficiency

### Color (Bayer RGB) with Microlens

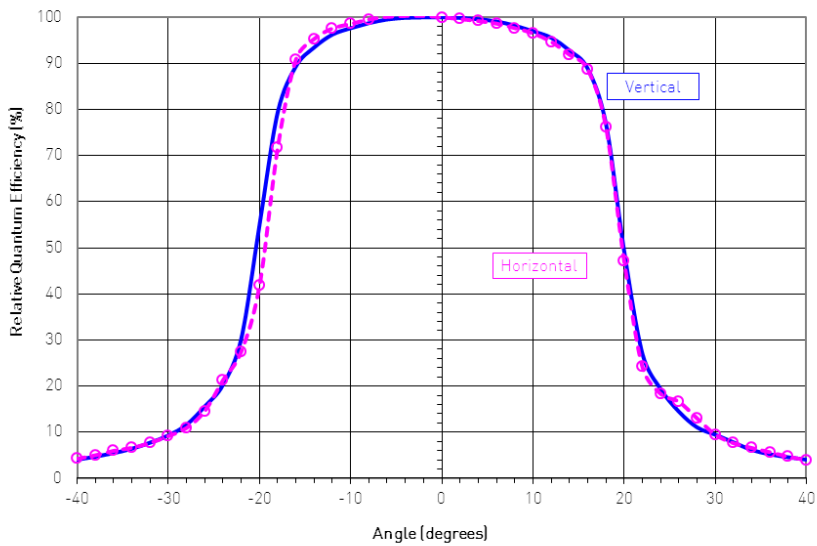


Figure 11: Color (Bayer RGB) with Microlens Angular Quantum Efficiency



### DARK CURRENT VERSUS TEMPERATURE

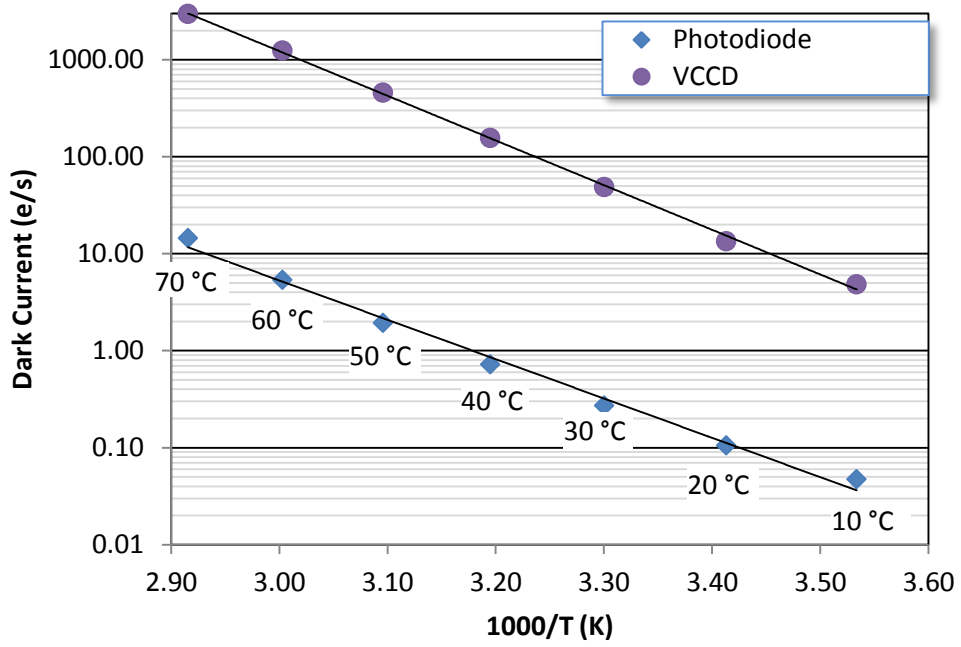


Figure 12: Dark Current versus Temperature



## POWER – ESTIMATED

### Power – Estimated – Full Resolution

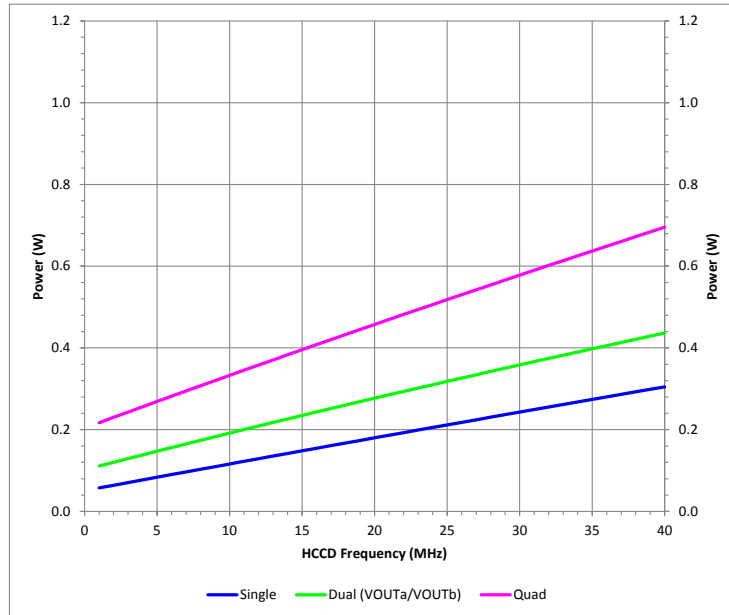


Figure 13: Power – Full Resolution

### Power – Estimated – 1/4 Resolution – 2x2 Binning

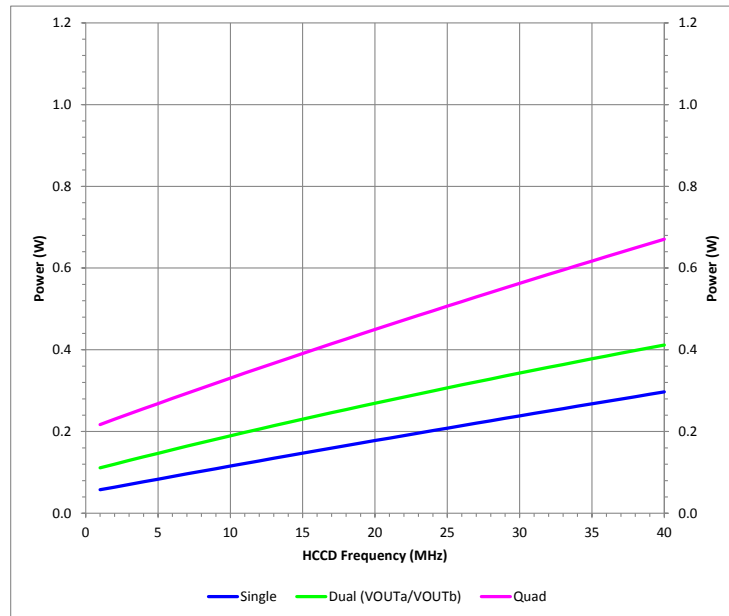


Figure 14: Power – 1/4 Resolution – Constant HCCD



### Power – 1/4 Resolution – 2x2 Binning using Variable HCCD XLDR

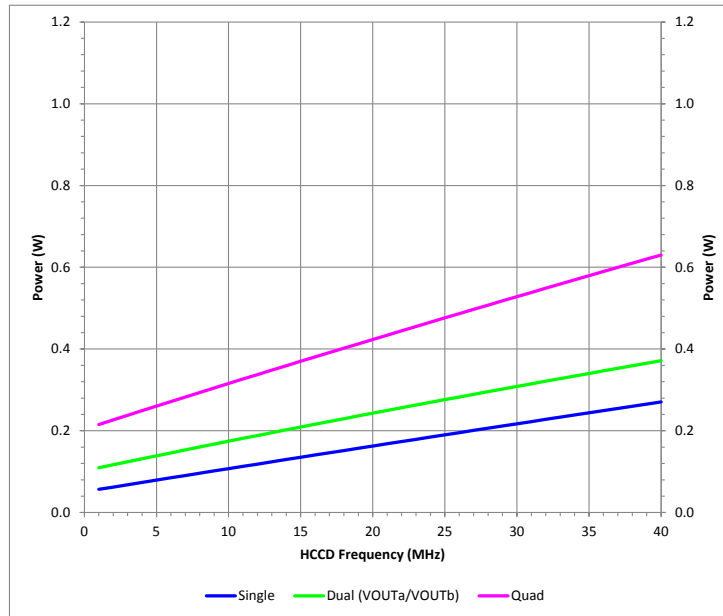


Figure 15: Power – 1/4 Resolution – Variable HCCD XLDR

### Power – 1/4 Resolution – 2x2 Binning using Constant XLDR

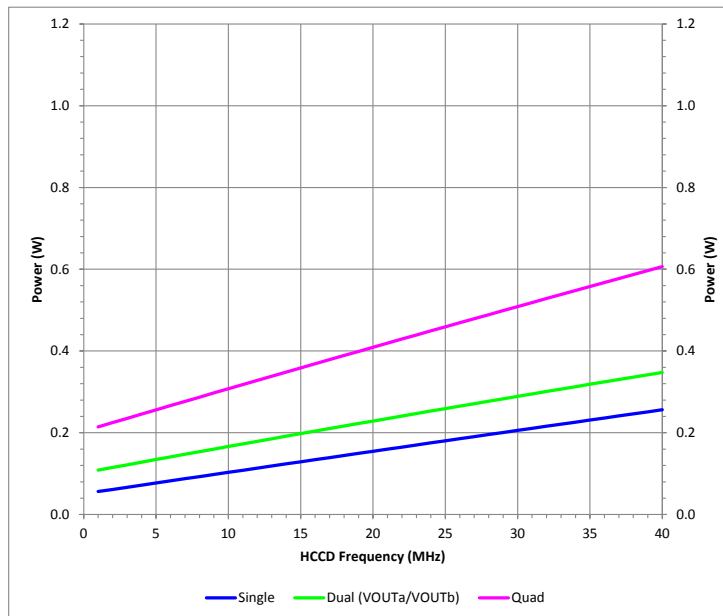


Figure 16: Power – 1/4 Resolution - Constant HCCD XLDR



## FRAME RATES

### Frame Rates – Full Resolution

Frame rates are for low and high gain modes of operation.

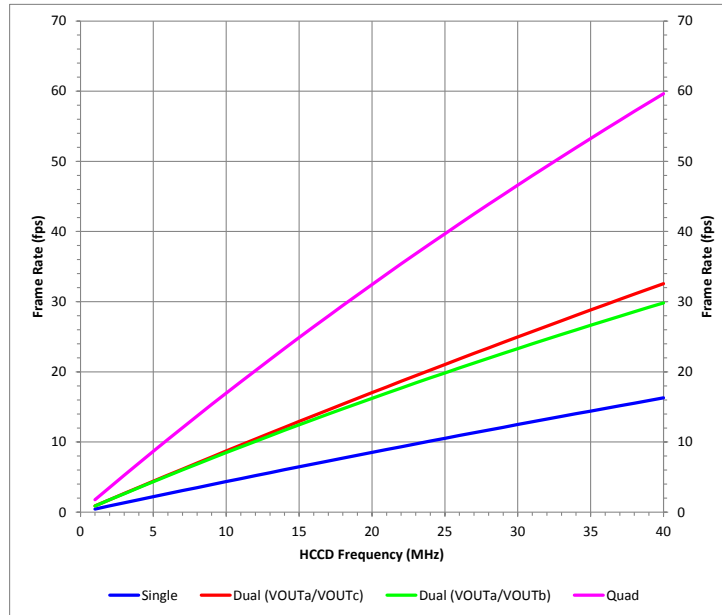


Figure 17: Frame Rates – Full Resolution

### Frame Rates – 1/4 Resolution – 2x2 Binning

Frame rates for low gain and high gain modes of operation

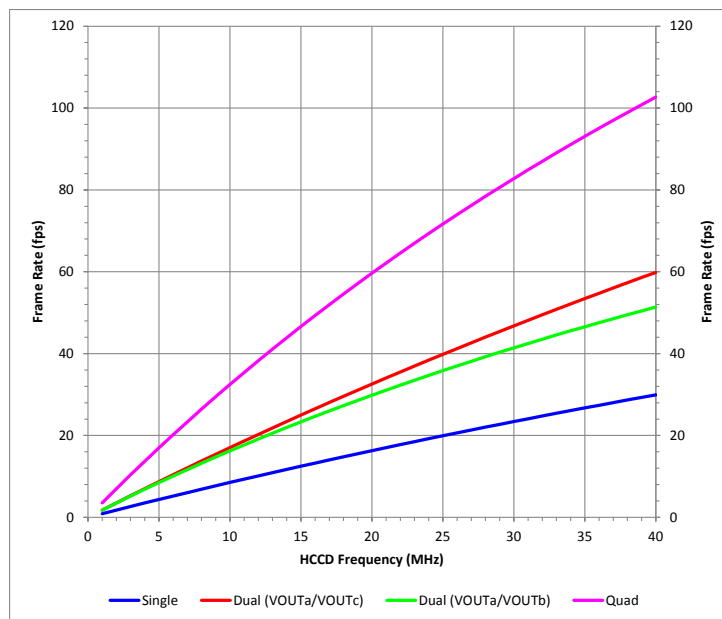


Figure 18: Frame Rates – 1/4 Resolution – Constant HCCD



### Frame Rates – 1/4 Resolution – 2x2 Binning using Variable HCCD XLDR

Frame rates for variable HCCD Modes of operation

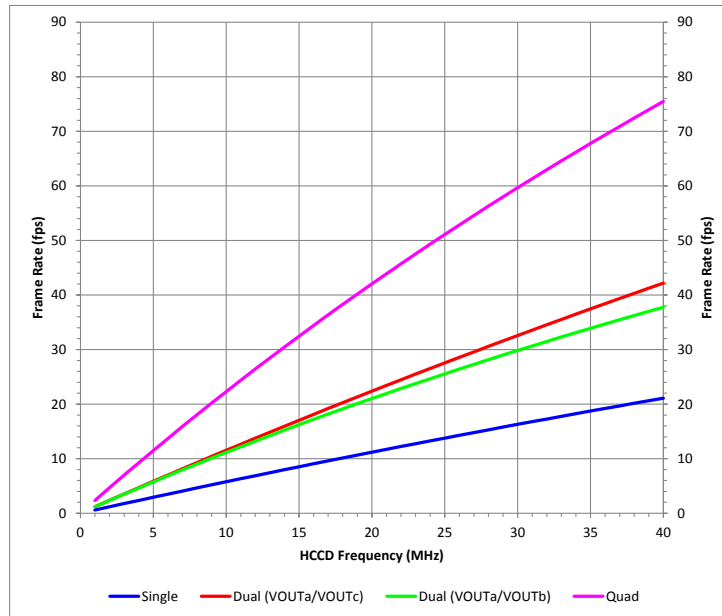


Figure 19: Frame Rates – 1/4 Resolution – Variable HCCD

### Frame Rates – 1/4 Resolution – 2x2 Binning using Constant XLDR

Frame rates for a constant HCCD mode of operation

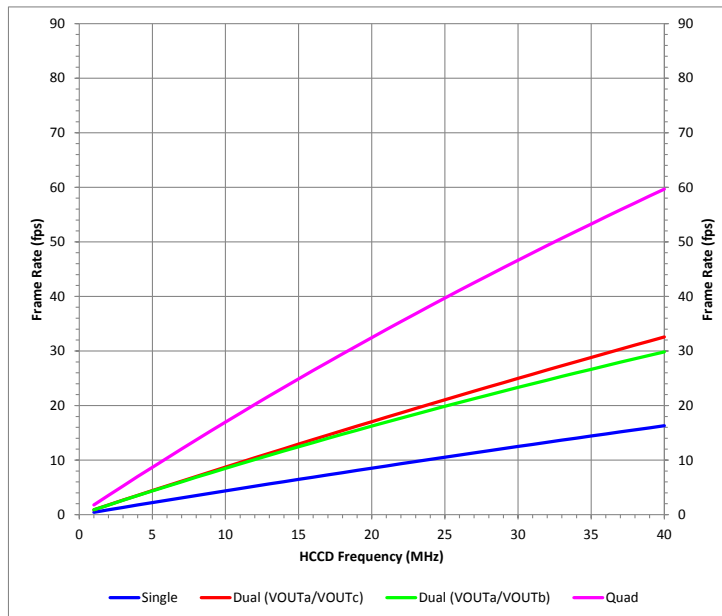


Figure 20: Frame Rates – 1/4 Resolution - Constant HCCD XLDR



## Defect Definitions

### OPERATION CONDITIONS FOR DEFECT TESTING AT 40 °C

Description	Condition	Notes
Operational Mode	One output, using VOUTa, continuous readout	
HCCD Clock Frequency	20 MHz	
Pixels Per Line	1992	
Lines Per Frame	1124	
Line Time	103.6 $\mu$ sec	
Frame Time	116.5 msec	
Photodiode Integration Time (PD_Tint)	PD_Tint = Frame Time = 116.5 msec, no electronic shutter used	
Temperature	40 °C	
Light Source	Continuous red, green and blue LED illumination	1
Operation	Nominal operating voltages and timing	

#### Notes

- For monochrome sensor, only the green LED is used.

### DEFECT DEFINITIONS FOR TESTING AT 40 °C

Description	Definition	Standard Grade	Notes
Major dark field defective bright pixel	Defect $\geq$ 40 mV	20	1
Major bright field defective pixel	-12% $\geq$ Defect $\geq$ +12%		
Minor dark field defective bright pixel	Defect $\geq$ 20 mV	200	
Cluster Defect	A group of 2 to 10 contiguous major defective pixels, but no more than 2 adjacent defects horizontally.	8	2
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	2

#### Notes:

- For the color devices (KAI-02170-CBA and KAI-02170-PBA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
- Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).





## OPERATION CONDITIONS FOR DEFECT TESTING AT 27 °C

Description	Condition	Notes
Operational Mode	One output, using VOUTa, continuous readout	
HCCD Clock Frequency	20 MHz	
Pixels Per Line	1992	
Lines Per Frame	1124	
Line Time	103.6 $\mu$ sec	
Frame Time	116.5 msec	
Photodiode Integration Time (PD_Tint)	PD_Tint = Frame Time = 116.5 msec, no electronic shutter used	
Temperature	27 °C	
Light Source	Continuous red, green and blue LED illumination	1
Operation	Nominal operating voltages and timing	

### Notes

1. For monochrome sensor, only the green LED is used.

## DEFECT DEFINITIONS FOR TESTING AT 27 °C

Description	Definition	Standard Grade	Notes
Major dark field defective bright pixel	Defect $\geq$ 13 mV	20	1
Major bright field defective pixel	-12% $\geq$ Defect $\geq$ +12%		
Cluster Defect	A group of 2 to 10 contiguous major defective pixels, but no more than 2 adjacent defects horizontally.	8	2
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	2

### Notes:

1. For the color devices (KAI-02170-CBA and KAI-02170-PBA), a bright field defective pixel deviates by 12 % with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

## Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27 °C) temperature. Minor point defects are not included in the defect map. All defective pixels are reference to pixel 1, 1 in the defect maps. See Figure 21 for the location of pixel 1, 1.



## Test Definitions

### Test Regions of Interest

Image Area ROI: Pixel (1, 1) to Pixel (1936, 1096)

Active Area ROI: Pixel (9, 9) to Pixel (1928, 1088)

Center ROI: Pixel (919, 499) to Pixel (1018, 598)

Only the Active Area ROI pixels are used for performance and defect tests.

## OVERCLOCKING

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 21 for a pictorial representation of the regions of interest.

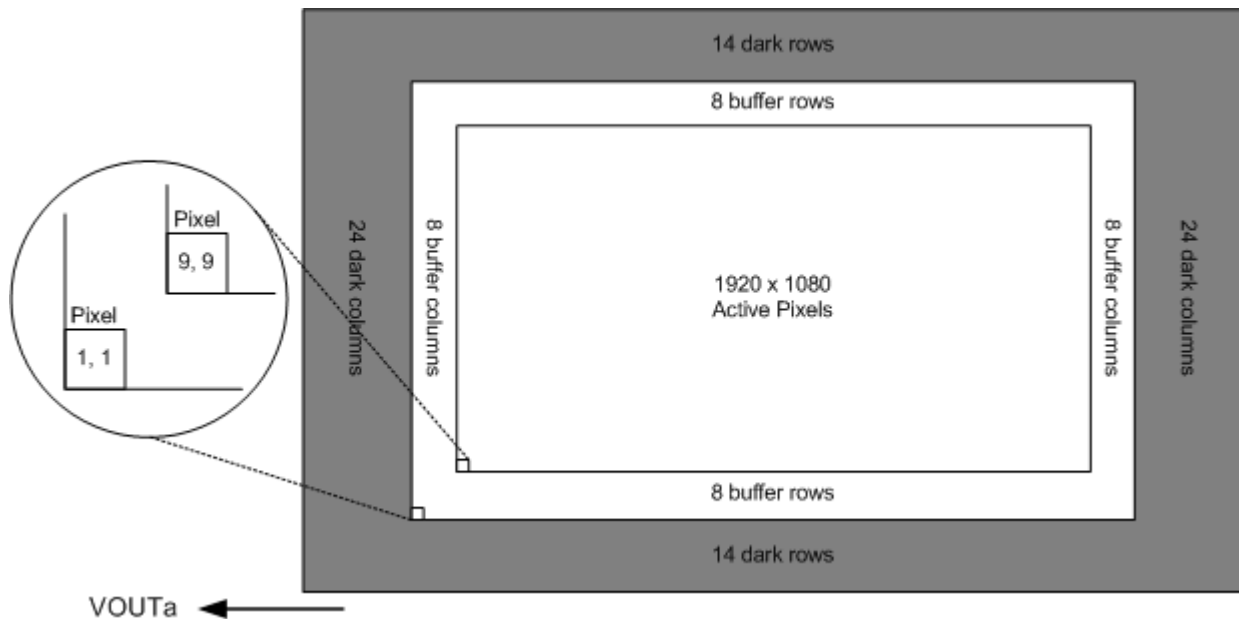


Figure 21: Regions of Interest



## TESTS

### Dark Field Global Non-Uniformity

This test is performed under dark field conditions. The sensor is partitioned into 144 sub regions of interest, each of which is 120 by 120 pixels in size. The average signal level of each of the 144 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$\text{Signal of ROI}[i] = (\text{ROI Average in counts} - \text{Horizontal overclock average in counts}) * \text{mV per count}$$

where  $i = 1$  to 144. During this calculation on the 144 sub regions of interest, the maximum and minimum signal levels are found. The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

Units: mVpp (millivolts peak to peak)

### Global Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1320 mV. Global non-uniformity is defined as

$$\text{GlobalNon-Uniformity} = 100 * \left( \frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}} \right)$$

Units: %rms. Active Area Signal = Active Area Average – Dark Column Average

### Global Peak to Peak Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1320 mV. The sensor is partitioned into 144 sub regions of interest, each of which is 120 by 120 pixels in size. The average signal level of each of the 144 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$\text{Signal of ROI}[i] = (\text{ROI Average in counts} - \text{Horizontal overclock average in counts}) * \text{mV per count}$$

Where  $i = 1$  to 144. During this calculation on the 144 sub regions of interest, the maximum and minimum signal levels are found. The global peak to peak uniformity is then calculated as:

$$\text{GlobalUniformity} = 100 * \frac{\text{MaximumSignal} - \text{MinimumSignal}}{\text{Active Area Signal}}$$

Units: %pp



## Center Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1320 mV. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels of the sensor. Center uniformity is defined as:

$$\text{Center ROI Uniformity} = 100 * \left( \frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}} \right)$$

Units: %rms. Center ROI Signal = Center ROI Average – Dark Column Average.

## Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 256 sub regions of interest, each of which is 120 by 120 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the “Defect Definitions” section.

## Bright Field Defect Test

This test is performed with the imager illuminated to a level such that the output is at approximately 924 mV. Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1320 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal \* threshold

Bright defect threshold = Active Area Signal \* threshold

The sensor is then partitioned into 144 sub regions of interest, each of which is 120 by 120 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

- Example for major bright field defective pixels:
- Average value of all active pixels is found to be 924 mV
- Dark defect threshold: 924 mV \* 12% = 111 mV
- Bright defect threshold: 924 mV \* 12% = 111 mV
- Region of interest #1 selected. This region of interest is pixels 9, 9 to pixels 128, 128
  - Median of this region of interest is found to be 920 mV
  - Any pixel in this region of interest that is  $\leq (920 - 111 \text{ mV})$  809 mV in intensity will be marked defective
  - Any pixel in this region of interest that is  $\geq (920 + 111 \text{ mV})$  1031 mV in intensity will be marked defective
- All remaining 144 sub regions of interest are analyzed for defective pixels in the same manner.



## Operation

### ABSOLUTE MAXIMUM RATINGS

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged. Operation at these values will reduce MTTF.

Description	Symbol	Minimum	Maximum	Units	Notes
Operating Temperature	$T_{OP}$	-50	+70	°C	1
Humidity	RH	+5	+90	%	2
Output Bias Current	$I_{out}$	-	60	mA	3
Off-chip Load	$C_L$	-	10	pF	

Notes:

- Noise performance will degrade at higher temperatures.
- $T=25$  °C. Excessive humidity will degrade MTTF.
- Total for all outputs. Maximum current is -15 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

### ABSOLUTE MAXIMUM VOLTAGE RATINGS BETWEEN PINS AND GROUND

Description	Minimum	Maximum	Units	Notes
VDDa, VOUTa	-0.4	17.5	V	1
RDa	-0.4	15.5	V	1
V1B, V1T	ESD - 0.4	ESD + 24.0	V	
V2B, V2T, V3B, V3T, V4B, V4T	ESD - 0.4	ESD + 14.0	V	
H1Sa, H1Ba, H2Sa, H2Ba, H2SLa, R1a, R2a, OGa	ESD - 0.4	ESD + 14.0	V	1
ESD	-10.0	0.0	V	
SUB	-0.4	+40.0	V	2

Notes:

- a denotes a, b, c or d
- Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*



### KAI-02150 COMPATIBILITY

The KAI-02170 is pin-for-pin compatible with a camera designed for the KAI-02150 image sensor under the following conditions:

- To operate in accordance with a system designed for KAI-02150, the target substrate voltage should be set to be 2.0 V higher than the value recorded on the KAI-02170 shipping container. This setting will cause the charge capacity to be limited to 20  $\mu\text{ke}^-$  (or 660 mV).
- On the KAI-02170, pins 17 (R2ab) and 51 (R2cd) should be left floating per the KAI-02150 Device Performance Specification.
- The KAI-02170 will operate in only the high gain mode (33  $\mu\text{V}/\text{e}^-$ ).
- All timing and voltages are taken from the KAI-02150 specification sheet.
- The number of horizontal and vertical CCD clock cycles is reduced as appropriate

In addition, if the intent is to operate the KAI-02170 image sensor in a camera designed for the KAI-02150 sensor that has been modified to accept and process the full 40,000  $\text{e}^-$  (1,320 mV) output, the following changes to the RD bias must be made:

Pins	Names	KAI-02150	KAI-02170
10, 26, 44, 60	RDa, RDb, RDc, RDd	12.0V per the specification	Increase to 12.6V

To make use of the low or dual gains modes the KAI-02170 voltages and timing specifications must be used.



### RESET PIN, LOW GAIN (R2AB AND R2CD)

The R2ab and R2bc (pins 17 and 51) each have an internal circuit to bias the pins to 4.3 V. This feature assures the device is set to operate in the high gain mode when pins 17 and 51 are not connected in the application to a clock driver (for KAI-02150 compatibility). Typical capacitor coupled drivers will not drive this structure.

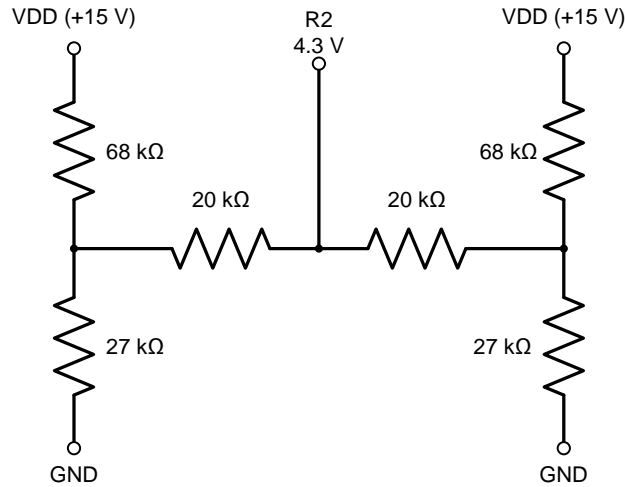


Figure 22: Equivalent Circuit for Reset Gate, low Gain (R2ab and R2cd)



## POWER UP AND POWER DOWN SEQUENCE

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor.

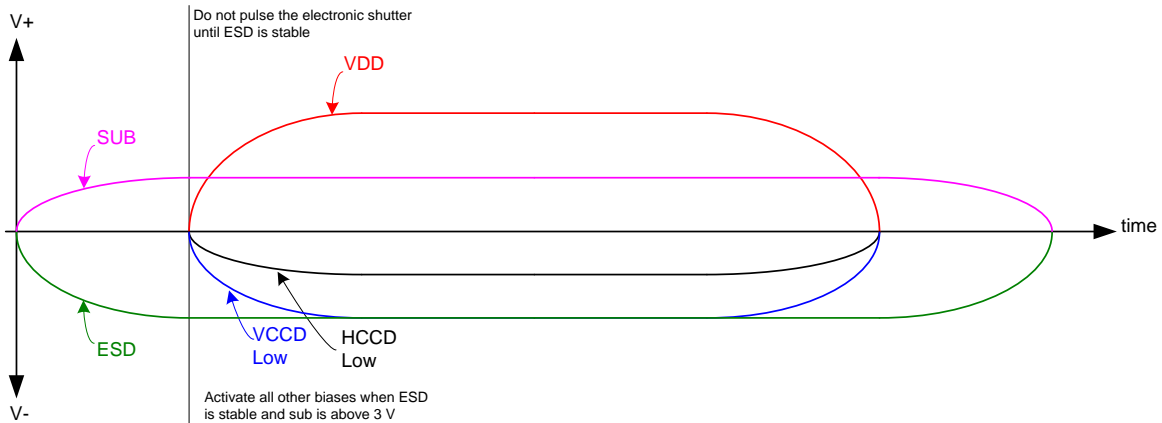
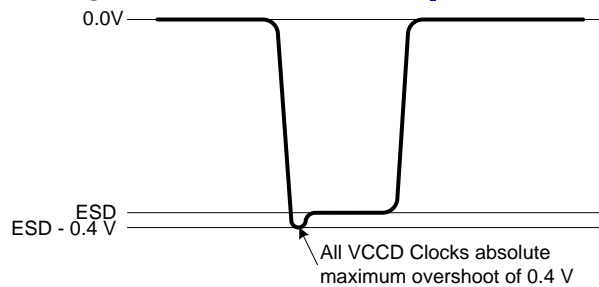


Figure 23: Power Up and Power Down Sequence

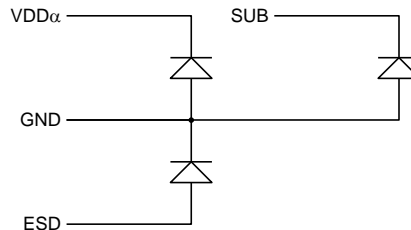
Notes:

1. Activate all other biases when ESD is stable and SUB is above 3 V
2. Do not pulse the electronic shutter until ESD is stable
3. VDD cannot be +15 V when SUB is 0 V
4. The image sensor can be protected from an accidental improper ESD voltage by current limiting the SUB current to less than 10 mA. SUB and VDD must always be greater than GND. ESD must always be less than GND. Placing diodes between SUB, VDD, ESD and ground will protect the sensor from accidental overshoots of SUB, VDD and ESD during power on and power off. See the figure below.

The VCCD clock waveform must not have a negative overshoot more than 0.4 V below the ESD voltage.



Example of external diode protection for SUB, VDD and ESD.  $\alpha$  denotes a, b, c or d.







## DC BIAS OPERATING CONDITIONS

Description	Pins	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current	Notes
Reset Drain	RD <sub>a</sub>	RD	+12.4	+12.6	+12.8	V	10 μA	1, 9
Output Gate	OG <sub>a</sub>	OG	-2.2	-2.0	-1.8	V	10 μA	1
Output Amplifier Supply	VDD <sub>a</sub>	VDD	+14.5	+15.0	+15.5	V	11.0 mA	1, 2
Ground	GND	GND	0.0	0.0	0.0	V	-1.0 mA	
Substrate	SUB	VSUB	+5.0	VAB	VDD	V	50 μA	3, 8
ESD Protection Disable	ESD	ESD	-9.2	-9.0	V <sub>x_L</sub>	V	50 μA	6, 7, 10
Output Bias Current	VOU <sub>Ta</sub>	I <sub>out</sub>	-3.0	-5.0	-10.0	mA	—	1, 4, 5

Notes:

1. a denotes a, b, c or d
2. The maximum DC current is for one output. I<sub>dd</sub> = I<sub>out</sub> + I<sub>ss</sub>. See Figure 24.
3. The operating value of the substrate voltage, VAB, will be marked on the shipping container for each device. The value of VAB is set such that the photodiode charge capacity is the nominal PNe (see Specifications).
4. An output load sink must be applied to each VOUT pin to activate each output amplifier.
5. Nominal value required for 40 MHz operation per output. May be reduced for slower data rates and lower noise.
6. Adherence to the power-up and power-down sequence is critical. See Power Up and Power Down Sequence section.
7. ESD maximum value must be less than or equal to V1\_L+0.4 V and V2\_L+0.4 V.
8. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.
9. 12.0 V may be used if the total output signal desired is 20,000 e<sup>-</sup> or less.
10. Where V<sub>x\_L</sub> is the level set for V1\_L, V2\_L, V3\_L, or V4\_L in the application.

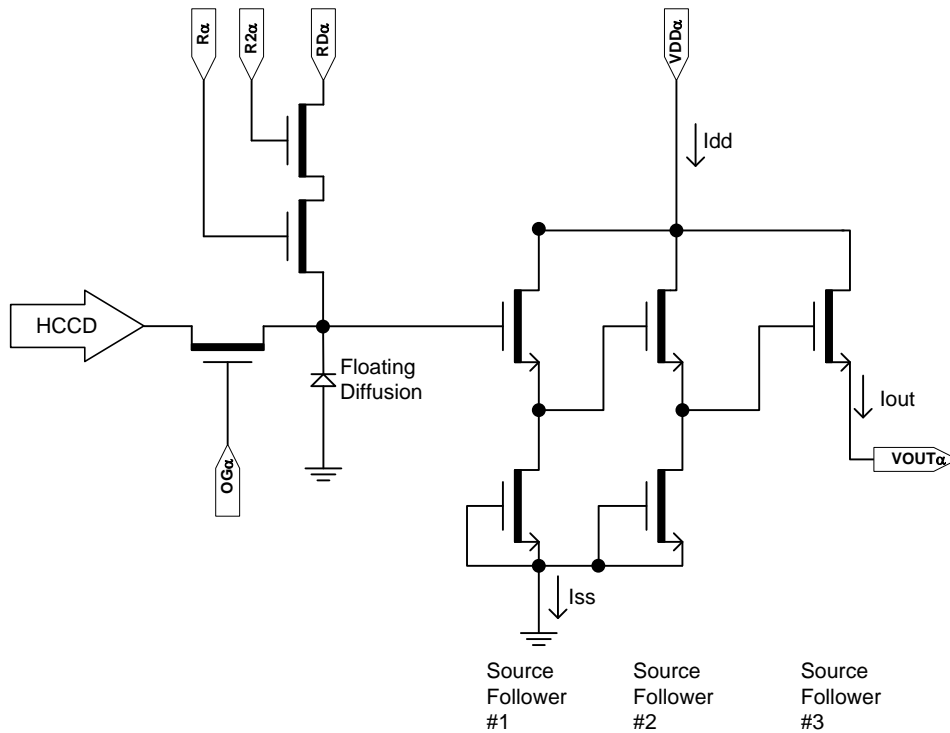


Figure 24: Output Amplifier



## AC OPERATING CONDITIONS

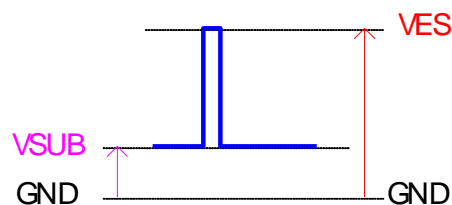
### Clock Levels

Description	Pins <sup>1</sup>	Symbol	Level	Minimum	Nominal	Maximum	Units
Vertical CCD Clock, Phase 1	V1B, V1T	V1_L	Low	-8.2	-8.0	-7.8	V
		V1_M	Mid	-0.2	+0.0	+0.2	
		V1_H	High	11.5	12.0	12.5	
Vertical CCD Clock, Phase 2	V2B, V2T	V2_L	Low	-8.2	-8.0	-7.8	V
		V2_H	High	-0.2	+0.0	+0.2	
Vertical CCD Clock, Phase 3	V3B, V3T	V3_L	Low	-8.2	-8.0	-7.8	V
		V3_H	High	-0.2	+0.0	+0.2	
Vertical CCD Clock, Phase 4	V4B, V4T	V4_L	Low	-8.2	-8.0	-7.8	V
		V4_H	High	-0.2	+0.0	+0.2	
Horizontal CCD Clock, Phase 1 Storage	H1Sa	H1S_L	Low	-5.2	-4.0	-3.8	V
		H1S_A	Amplitude <sup>3</sup>	+3.8	+4.0	+5.2	
Horizontal CCD Clock, Phase 1 Barrier	H1Ba	H1B_L	Low	-5.2	-4.0	-3.8	V
		H1B_A	Amplitude <sup>3</sup>	+3.8	+4.0	+5.2	
Horizontal CCD Clock, Phase 2 Storage	H2Sa	H2S_L	Low	-5.2	-4.0	-3.8	V
		H2S_A	Amplitude <sup>3</sup>	+3.8	+4.0	+5.2	
Horizontal CCD Clock, Phase 2 Barrier	H2Ba	H2B_L	Low	-5.2	-4.0	-3.8	V
		H2B_A	Amplitude <sup>3</sup>	+3.8	+4.0	+5.2	
Horizontal CCD Clock, Last Phase <sup>2</sup>	H2SLa	H2SL_L	Low	-5.2	-5.0	-4.8	V
		H2SL_A	Amplitude <sup>3</sup>	+4.8	+5.0	+5.2	
Reset Gate	R1a	R_L	Low	-3.2	-3.0	-2.8	V
		R_A	Amplitude	+6.0	—	+6.4	
Reset Gate 2	R2a	R2_L	Low	-2.0	-1.8	-1.6	V
		R2_A	Amplitude	+6.0	—	+6.4	
Electronic Shutter <sup>4</sup>	SUB	VES	High	+29.0	+30.0	+40.0	V

Notes:

1. a denotes a, b, c or d
2. Use separate clock driver for improved speed performance.
3. The horizontal clock amplitude should be set such that the high level reaches 0.0 volts. Examples:
  - a. If the minimum horizontal low voltage of -5.2 V is used, then a 5.2 volt amplitude clock is required for a clock swing of -5.2 V to 0.0 V
  - b. If the maximum horizontal low voltage of -3.8 V is used, then a 3.8 volt amplitude clock is required for a clock swing of -3.8 V to 0.0 V
4. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

The figure below shows the DC bias (VSUB) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.





## Capacitance

	V1B	V2B	V3B	V4B	V1T	V2T	V3T	V4T	GND	All Pins	Units
V1B		2.2	1.5	1.8	0.8	0.7	0.8	0.5	3.2	11.6	nF
V2B			2.8	1.3	0.7	0.4	0.5	0.4	0.9	9.8	nF
V3B				2.5	0.8	0.7	0.8	0.5	1.1	10.9	nF
V4B					0.7	0.5	0.7	0.4	3.0	10.0	nF
V1T						1.8	1.5	2.2	3.2	11.3	nF
V2T							2.1	0.8	2.9	9.9	nF
V3T								2.5	1.5	11.1	nF
V4T									0.7	9.6	nF
VSub	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	1.5	1.5	nF

	H2S	H1B	H2B	GND	All Pins	Units
H1S	15	25	15	65	120	pF
H2S		16	14	94	123	pF
H1B			4	105	108	pF
H2B				98	98	pF

### Notes

1. Tables show typical cross capacitance between pins of the device
2. Capacitance is total for all like pins
3. Capacitance values are estimated



## DEVICE IDENTIFICATION

The device identification pin (DevID) may be used to determine which Truesense Imaging 7.4 micron pixel interline CCD sensor is being used.

Description	Pins	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current	Notes
Device Identification	DevID	DevID	14,000	16,000	18,000	Ohms	50 $\mu$ A	1, 2, 3

Notes:

1. Nominal value subject to verification and/or change during release of preliminary specifications.
2. If the Device Identification is not used, it may be left disconnected.
3. After Device Identification resistance has been read during camera initialization, it is recommended that the circuit be disabled to prevent localized heating of the sensor due to current flow through the R\_DeviceID resistor.

## Recommended Circuit

Note that V1 must be a different value than V2.

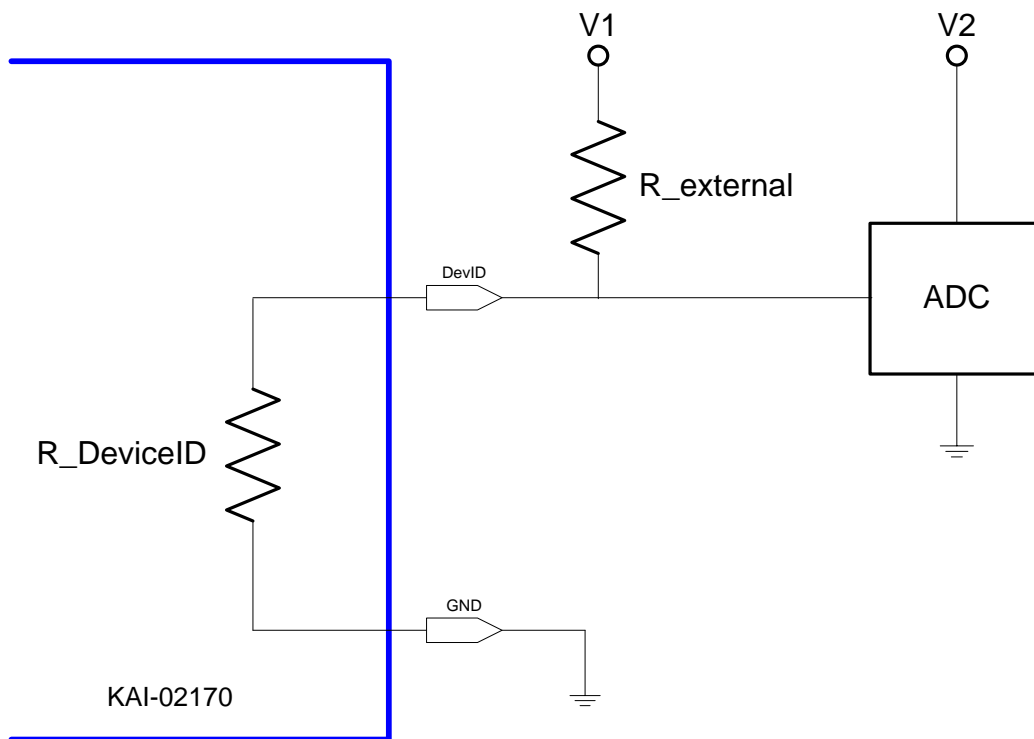


Figure 25: Device Identification Recommended Circuit



## Timing

### REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Photodiode Transfer	Tpd	1.0	-	-	μs	
VCCD Leading Pedestal	T3p	4.0	-	-	μs	
VCCD Trailing Pedestal	T3d	4.0	-	-	μs	
VCCD Transfer Delay	Td	1.0	-	-	μs	
VCCD Transfer	Tv	1.2	-	-	μs	
VCCD Clock Cross-over	Vvcr	75	-	100	%	1
VCCD Rise, Fall Times	Tvr, Tvf	5	-	10	%	1, 2
HCCD Delay	Ths	2.0	-	-	μs	
HCCD Transfer	Te	25.0	-	-	ns	
Shutter Transfer	Tsub	1.0	-	-	μs	
Shutter Delay	Thd	1.0	-	-	μs	
Reset Pulse	Tr	2.5	-	-	ns	
Reset – Video Delay	Trv	-	2.2	-	ns	
H2SL – Video Delay	Thv	-	3.1	-	ns	
Line Time	Tline	29.8	-	-	μs	Dual HCCD Readout
		54.6	-	-		Single HCCD Readout
Frame Time	Tframe	16.8	-	-	ms	Quad HCCD Readout
		33.5	-	-		Dual HCCD Readout
		61.4	-	-		Single HCCD Readout
Line Time (XLDR Bin 2x2)	Tline	59.6	-	-	μs	Dual HCCD Readout
		109.2	-	-		Single HCCD Readout
Frame Time (XLDR Bin 2x2) Constant HCCD timing <sup>3</sup>	Tframe	16.8	-	-	ms	Quad HCCD Readout
		33.5	-	-		Dual HCCD Readout
		61.4	-	-		Single HCCD Readout
Frame Time (XLDR Bin 2x2) Variable HCCD timing	Tframe	13.3	-	-	ms	Quad HCCD Readout
		26.5	-	-		Dual HCCD Readout
		47.4	-	-		Single HCCD Readout

#### Notes:

1. Refer to Figure 43: VCCD Clock Rise Time, Fall Time, and Edge Alignment
2. Relative to the VCCD Transfer pulse width, Tv



## TIMING FLOW CHARTS

In the timing flow charts the number of HCCD clock cycles per row, NH, and the number of VCCD clock cycles per frame, NV, are shown in the following table

	Full Resolution		1/4 Resolution		XLDR	
	NV	NH	NV	NH	NV	NH
Quad	562	1004	281	502	281	502
Dual VOUTa, VOUTc	562	2008	281	1004	281	1004
Dual VOUTa, VOUTb	1124	1004	562	502	562	502
Single VOUTa	1124	2008	562	1004	562	1004

Table 1: Values for NH and NV When Operating the Sensor in the Various Modes of Resolution

Notes:

1. The time to read out one line  $T_{line} = \text{Line Timing} + NH / (\text{pixel frequency})$ .
2. The time to read out one frame  $T_{frame} = NV * T_{line} + \text{Frame Timing}$ .
3. Line Timing: See Table 3: Line Timing.
4. Frame Timing: See Table 2: Frame Timing.
5. XLDR: eXtended Linear Dynamic Range.

### No Electronic Shutter

In this case the photodiode exposure time is equal to the time to read out an image. This flow chart applies to both full and 1/4 resolution modes.

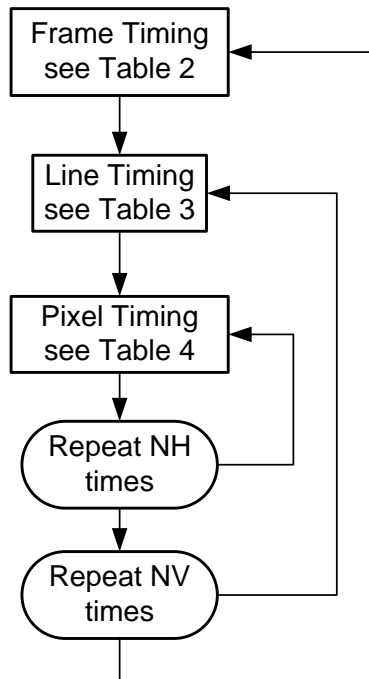


Figure 26: Timing Flow When Electronic Shutter is Not Used



### Using the Electronic Shutter

This flow chart applies to both the full and 1/4 resolution modes. The exposure time begins on the falling edge of the electronic shutter pulse on the SUB pin. The exposure time ends on the falling edge of the photodiode transfer (Tpd) of the V1T and V1B pins. The electronic shutter timing is shown in Figure 34.

NEXP: Exposure time in increments of number of lines.

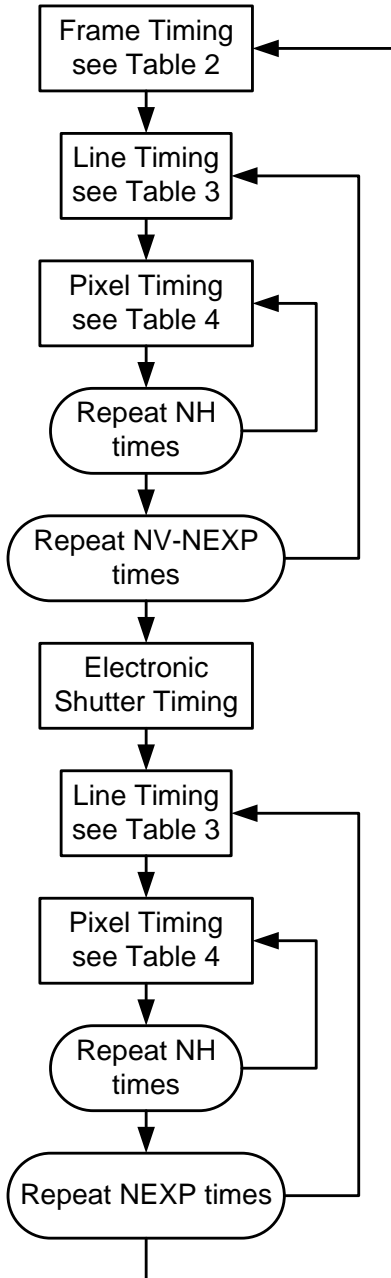


Figure 27: Timing Flow Chart Using the Electronic Shutter for Exposure Control



## TIMING TABLES

### Frame Timing

This timing table is for transferring charge from the photodiodes to the VCCD. See Figure 28 and Figure 29 for frame timing diagrams.

Device Pin	Full Resolution, high gain OR low gain				1/4 Resolution, high gain OR low gain				1/4 Resolution XLDR			
	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa
V1T	F1T		F1B	F1B	F1T		F1B		F1T		F1B	
V2T	F2T		F4B	F4B	F2T		F4B		F2T		F4B	
V3T	F3T		F3B	F3B	F3T		F3B		F3T		F3B	
V4T	F4T		F2B	F2B	F4T		F2B		F4T		F2B	
V1B	F1B				F1B				F1B			
V2B	F2B				F2B				F2B			
V3B	F3B				F3B				F3B			
V4B	F4B				F4B				F4B			
H1Sa	P1				P1Q				P1XL			
H1Ba	P1				P1Q				P1XL			
H2Sa	P2				P2Q				P2XL			
H2Ba	P2				P2Q				P2XL			
Ra	RHG/RLG				RHGQ/RLGQ				RXL			
H1Sb	P1				P1Q				P1XL			
H1Bb	P1	P2	P1	P2	P1Q	P2Q	P1Q	P2Q	P1XL	P2XL	P1XL	P2XL
H2Sb	P2				P2Q				P2XL			
H2Bb	P2	P1	P2	P1	P2Q	P1Q	P2Q	P1Q	P2XL	P1XL	P2XL	P1XL
Rb	RHG/RLG	Note 1	RHG/RLG	Note 1	RHGQ/RLGQ	Note 1	RHGQ/RLGQ	Note 1	RXL	Note 1	RXL	Note 1
R2ab	R2HG/R2LG				R2HGQ/R2LGQ				R2XL			
H1Sc	P1		Note 1		P1Q		Note 1		P1XL		Note 1	
H1Bc	P1		Note 1		P1Q		Note 1		P1XL		Note 1	
H2Sc	P2		Note 1		P2Q		Note 1		P2XL		Note 1	
H2Bc	P2		Note 1		P2Q		Note 1		P2XL		Note 1	
Rc	RHG/RLG		Note 1		RHGQ/RLGQ		Note 1		RXL		Note 1	
H1Sd	P1		Note 1		P1Q		Note 1		P1XL		Note 1	
H1Bd	P1	P2	Note 1		P1Q	P2Q	Note 1		P1XL	P2XL	Note 1	
H2Sd	P2		Note 1		P2Q		Note 1		P2XL		Note 1	
H2Bd	P2	P1	Note 1		P2Q	P1Q	Note 1		P2XL	P1XL	Note 1	
Rd	RHG/RLG	Note 1			RHGQ/RLGQ	Note 1			RXL	Note 1		
R2cd	R2HG/R2LG		Note 1		R2HGQ/R2LGQ		Note 1		R2XL		Note 1	
SHP (2)	SHP1				SHPQ				Note 4			
SHD (2)	SHD1				SHDQ				Note 5			

Table 2: Frame Timing

Notes:

1. This clock should be held at its high level voltage (0\_V) or held at +5.0\_V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor
3. This note intentionally left empty
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal





### Line Timing

This timing is for transferring one line of charge from the VCCD to the HCCD. See Figure 30, Figure 31, Figure 32 and Figure 33 for line timing diagrams.

Device Pin	Full Resolution, high gain OR low gain				1/4 Resolution, high gain OR low gain				1/4 Resolution XLDR			
	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa
V1T	L1T		L1B		2x L1T		2x L1B		2x L1T		2x L1B	
V2T	L2T		L4B		2x L2T		2x L4B		2x L2T		2x L4B	
V3T	L3T		L3B		2x L3T		2x L3B		2x L3T		2x L3B	
V4T	L4T		L2B		2x L4T		2x L2B		2x L4T		2x L2B	
V1B	L1B				2x L1B				2x L1B			
V2B	L2B				2x L2B				2x L2B			
V3B	L3B				2x L3B				2x L3B			
V4B	L4B				2x L4B				2x L4B			
H1Sa	P1L				P1LQ				P1XL			
H1Ba	P1L				P1LQ				P1XL			
H2Sa	P2L				P2LQ				P2XL			
H2Ba	P2L				P2LQ				P2XL			
Ra	RHG/RLG				RHGQ/RLGQ				RXL			
H1Sb	P1L				P1LQ				P1XL			
H1Bb	P1L	P2L	P1L	P2L	P1LQ	P2LQ	P1LQ	P2LQ	P1XL	P2XL	P1XL	P2XL
H2Sb	P2L				P2LQ				P2XL			
H2Bb	P2L	P1L	P2L	P1L	P2LQ	P1LQ	P2LQ	P1LQ	P2XL	P1XL	P2XL	P1XL
Rb	RHG/RLG	Note 1	RHG/RLG	Note 1	RHGQ/RLGQ	Note 1	RHGQ/RLGQ	Note 1	RXL	Note 1	RXL	Note 1
R2ab	R2HG/R2LG				R2HGQ/R2LGQ				R2XL			
H1Sc	P1L		Note 1		P1LQ		Note 1		P1XL		Note 1	
H1Bc	P1L		Note 1		P1LQ		Note 1		P1XL		Note 1	
H2Sc	P2L		Note 1		P2LQ		Note 1		P2XL		Note 1	
H2Bc	P2L		Note 1		P2LQ		Note 1		P2XL		Note 1	
Rc	RHG/RLG		Note 1		RHGQ/RLGQ		Note 1		RXL		Note 1	
H1Sd	P1L		Note 1		P1LQ		Note 1		P1XL		Note 1	
H1Bd	P1L	P2L	Note 1		P1LQ	P2LQ	Note 1		P1XL	P2XL	Note 1	
H2Sd	P2L		Note 1		P2LQ		Note 1		P2XL		Note 1	
H2Bd	P2L	P1L	Note 1		P2LQ	P1LQ	Note 1		P2XL	P1XL	Note 1	
Rd	RHG/RLG	Note 1		RHGQ/RLGQ		Note 1		RXL	Note 1			
R2cd	R2HG/R2LG		Note 1		R2HGQ/R2LGQ		Note 1		R2XL		Note 1	
SHP (2)	SHP1				SHPQ				Note 4			
SHD (2)	SHD1				SHDQ				Note 5			

Table 3: Line Timing

Notes:

1. This clock should be held at its high level voltage (0\_V) or held at +5.0\_V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor
3. The notation 2x L1B means repeat the L1B timing twice for every line. This sums two rows into the HCCD.
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal



### Pixel Timing

This timing is for transferring one pixel from the HCCD to the output amplifier.

Device Pin	Full Resolution, high gain OR low gain				1/4 Resolution, high gain OR low gain				1/4 Resolution XLDR			
	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa
V1T		-9V				-9V				-9V		
V2T		-9V				-9V				-9V		
V3T		0V				0V				0V		
V4T		0V				0V				0V		
V1B		-9V				-9V				-9V		
V2B		0V				0V				0V		
V3B		0V				0V				0V		
V4B		-9V				-9V				-9V		
H1Sa		P1				P1Q				P1XL		
H1Ba		P1				P1Q				P1XL		
H2Sa		P2				P2Q				P2XL		
H2Ba		P2				P2Q				P2XL		
Ra		RHG/RLG				RHGQ/RLGQ				RXL		
H1Sb		P1				P1Q				P1XL		
H1Bb	P1	P2	P1	P2	P1Q	P2Q	P1Q	P2Q	P1XL	P2XL	P1XL	P2XL
H2Sb		P2				P2Q				P2XL		
H2Bb	P2	P1	P2	P1	P2Q	P1Q	P2Q	P1Q	P2XL	P1XL	P2XL	P1XL
Rb	RHG/RLG	Note 1	RHG/RLG	Note 1	RHGQ/RLGQ	Note 1	RHGQ/RLGQ	Note 1	RXL	Note 1	RXL	Note 1
R2ab		R2HG/R2LG				R2HGQ/R2LGQ				R2XL		
H1Sc	P1		Note 1		P1Q		Note 1		P1XL		Note 1	
H1Bc	P1		Note 1		P1Q		Note 1		P1XL		Note 1	
H2Sc	P2		Note 1		P2Q		Note 1		P2XL		Note 1	
H2Bc	P2		Note 1		P2Q		Note 1		P2XL		Note 1	
Rc		RHG/RLG				RHGQ/RLGQ				RXL		
H1Sd		P1				P1Q				P1XL		
H1Bd	P1	P2	Note 1		P1Q	P2Q	Note 1		P1XL	P2XL	Note 1	
H2Sd		P2				P2Q				P2XL		
H2Bd	P2	P1	Note 1		P2Q	P1Q	Note 1		P2XL	P1XL	Note 1	
Rd	RHQ/RLG	Note 1			RHGQ/RLGQ	Note 1			RXL	Note 1		
R2cd		R2HG/R2LG				R2HGQ/R2LGQ				R2XL		
SHP (2)		SHP1				SHPQ				Note 4		
SHD (2)		SHD1				SHDQ				Note 5		

Table 4: Pixel Timing

Notes:

1. This clock should be held at its high level voltage (0\_V) or held at +5.0\_V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor
3. This note intentionally left empty
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal



### TIMING DIAGRAMS

The charge in the photodiodes is transferred to the VCCD on the rising edge of the +12 V pulse and is completed by the falling edge of the +12 V pulse. During the time period when F1T and F1B are at +12 V (Tpd) antiblooming protection is disabled. The photodiode integration time ends on the falling edge of the +12 V pulse.

See Table 2 for pin assignments.

### Frame Timing – Quadrant and Dual VOUTa/VOUTc Readout Modes

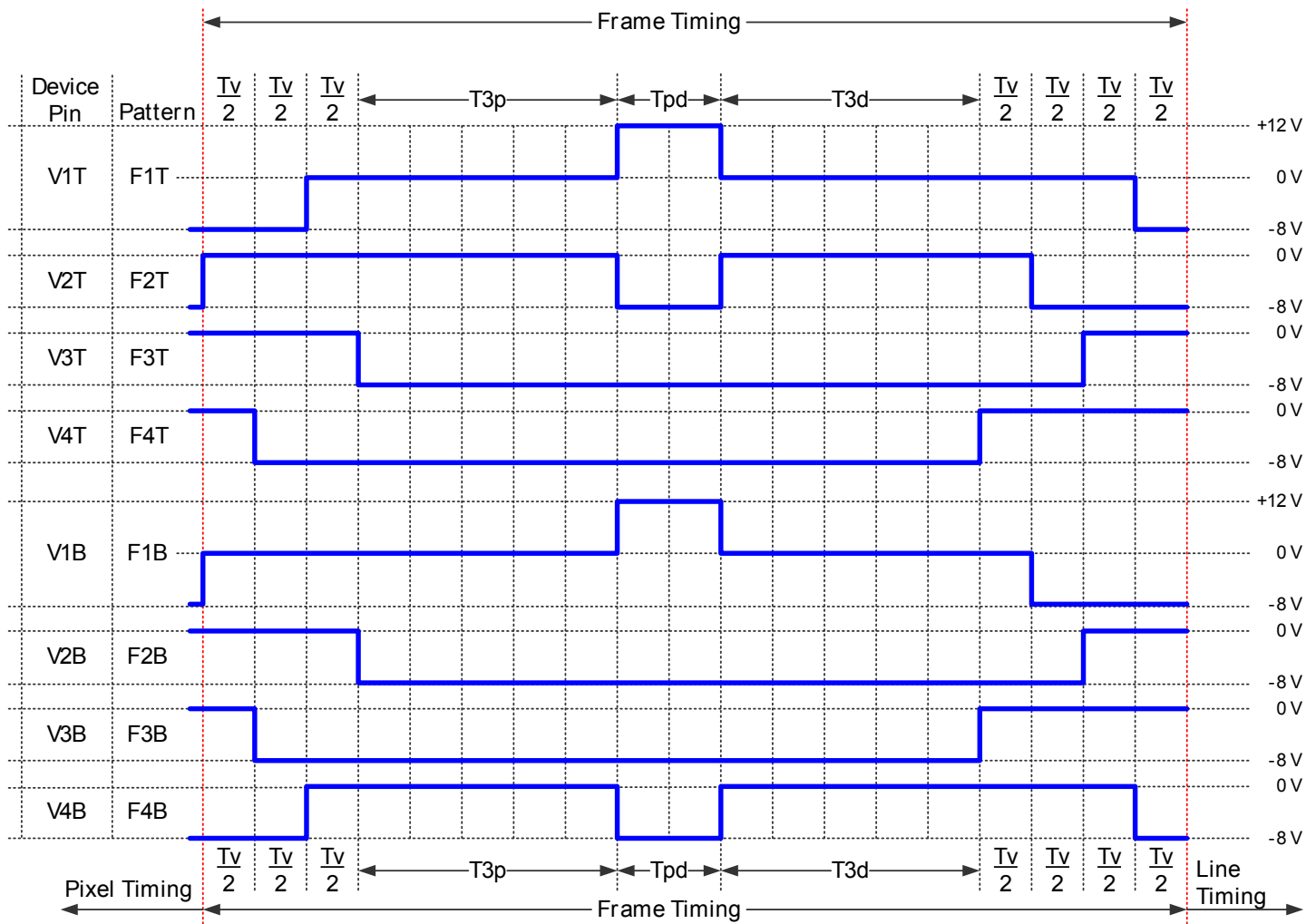


Figure 28: Frame Timing Diagram Quadrant and Dual VOUTa/VOUTc Readout Modes



### Frame Timing – Single and Dual VOUTa/VOUTb Readout Modes

See Table 2 for pin assignments.

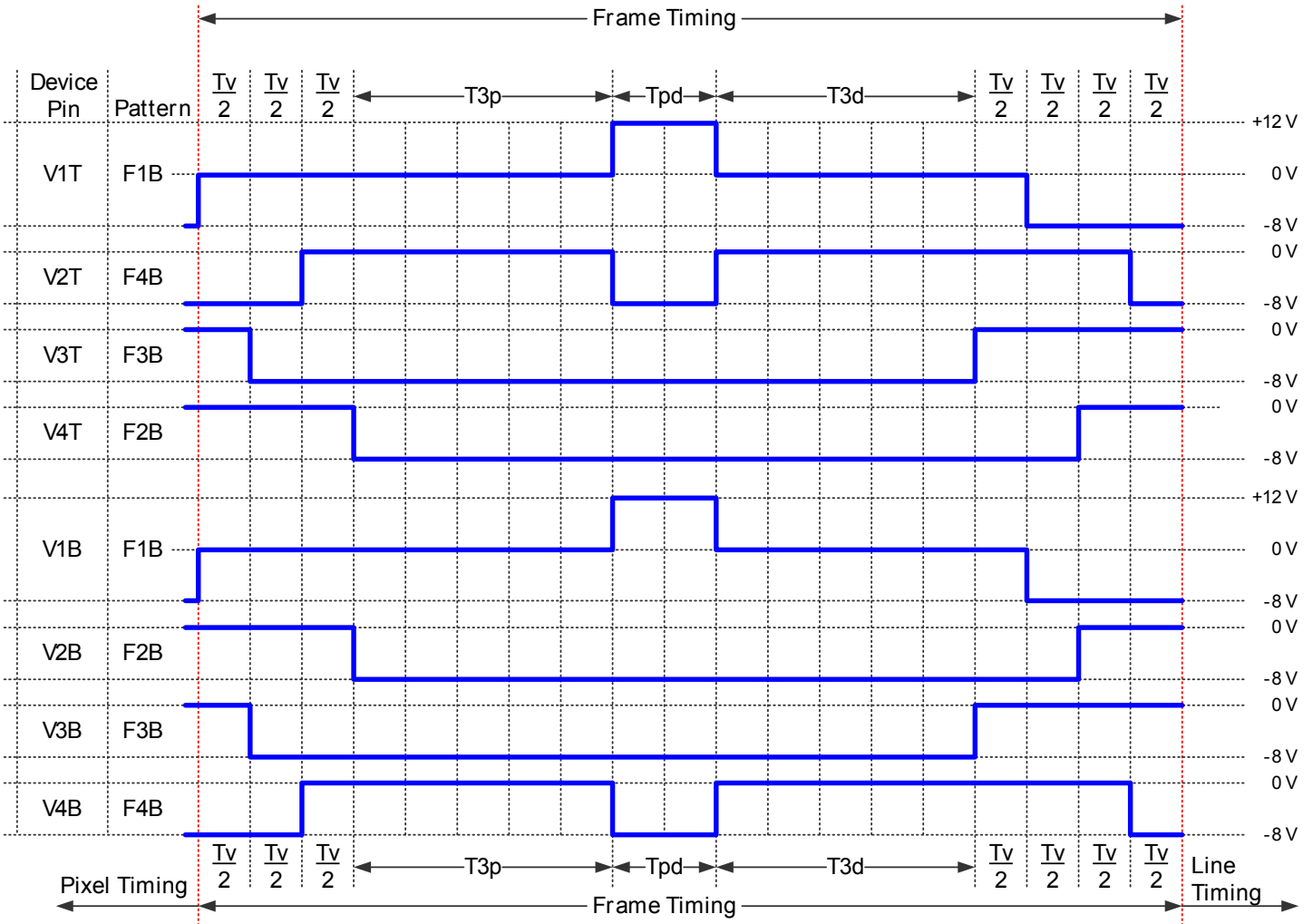


Figure 29: Frame Timing Diagram Single and Dual VOUTa/VOUTb Readout Modes



### Line Timing – Full Resolution – Quadrant and Dual VOUTa/VOUTc Readout Modes

See Table 3 for device pin assignments.

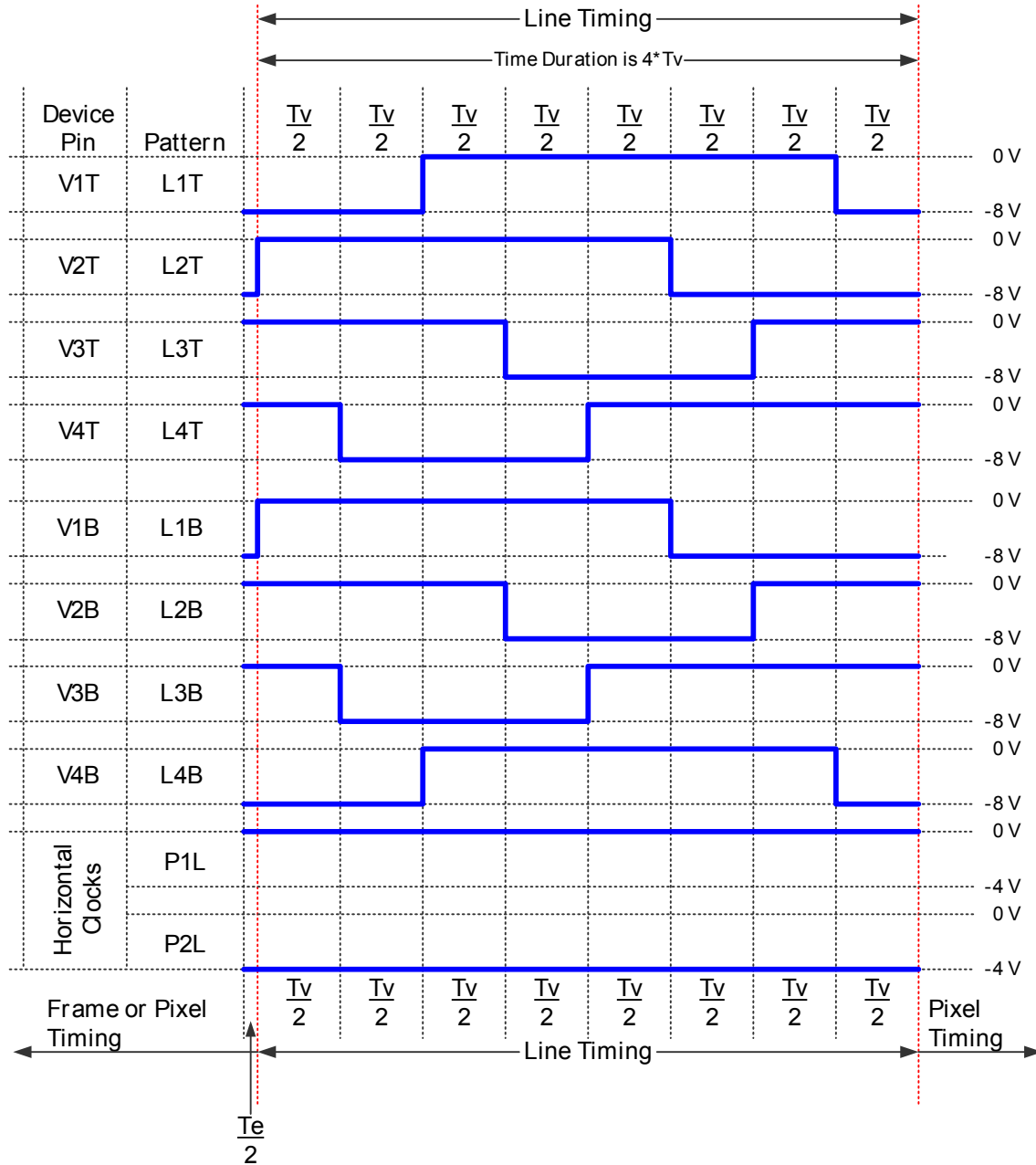


Figure 30: Line Timing Diagram – Full Resolution – Quadrant and Dual VOUTa/VOUTc Modes



### Line Timing – Full Resolution – Single and Dual VOUTa/VOUTb Readout Modes

See Table 3 for device pin assignments.

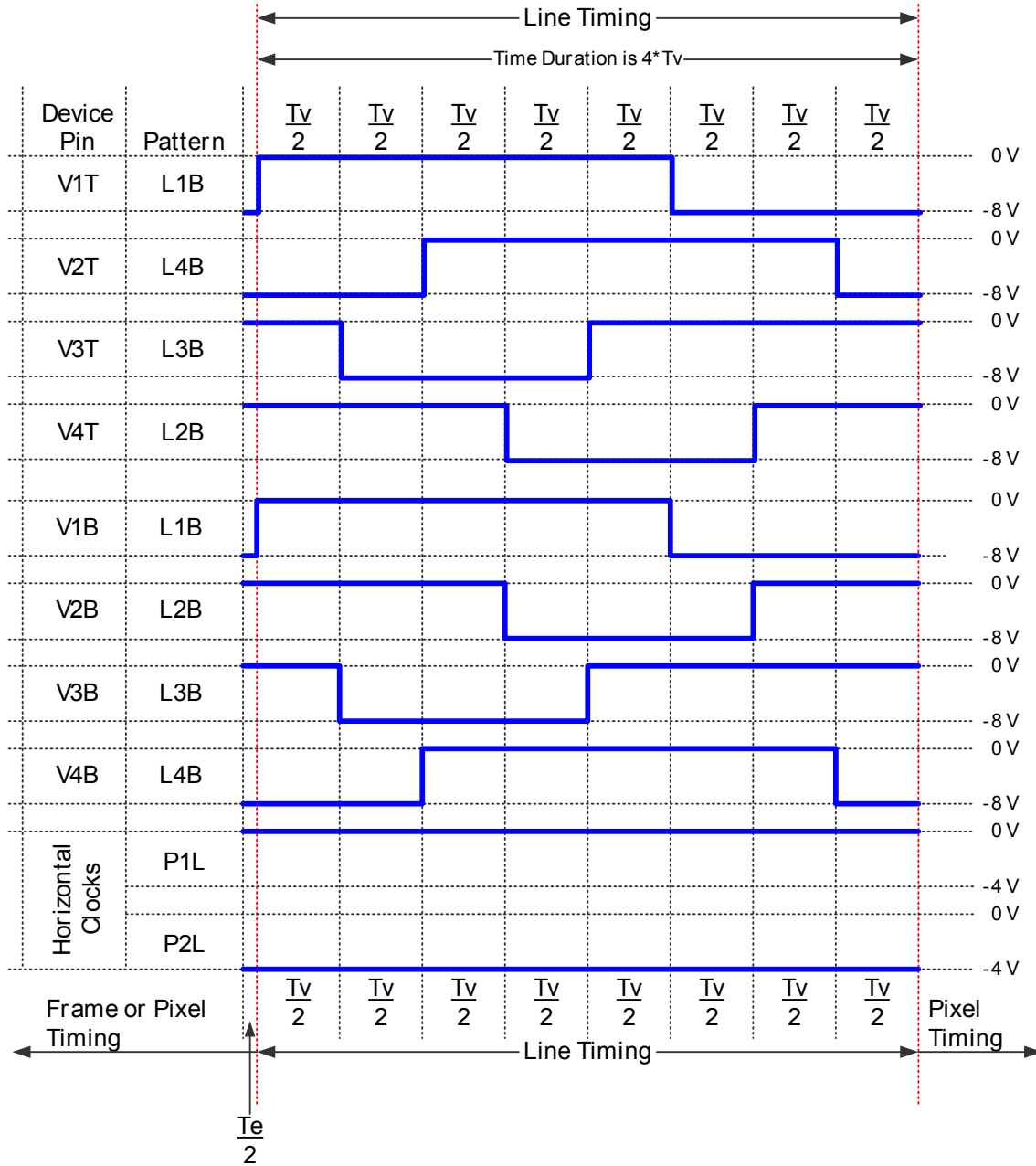


Figure 31: Line Timing Diagram – Full Resolution – Single and Dual VOUTa/VOUTb Modes



### Line Timing – Low Gain, High Gain and XLDR 1/4 Resolution – Quadrant and Dual VOUTa/VOUTc Readout Modes

See Table 3 for device pin assignments

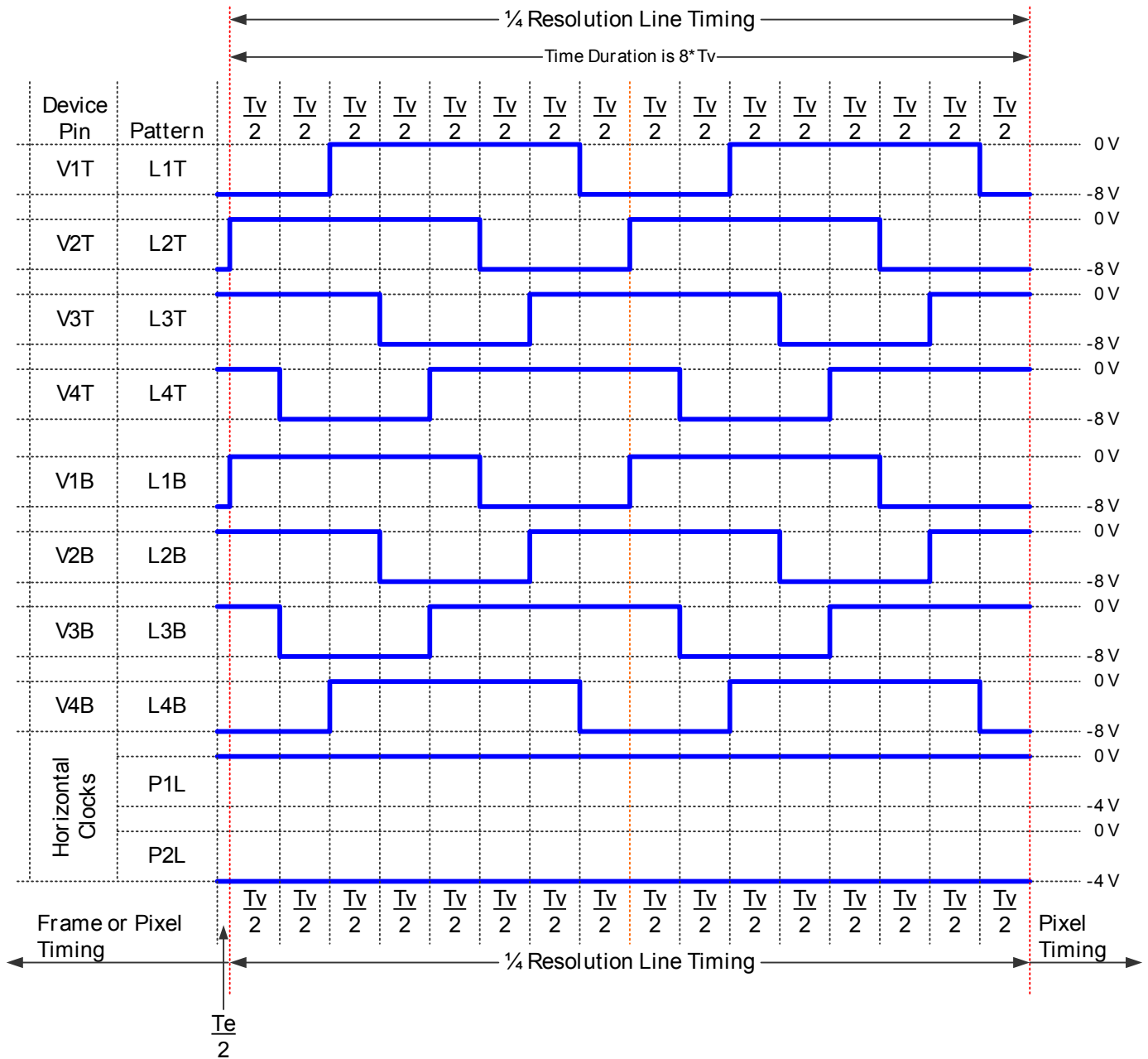


Figure 32: Line Timing Diagram – 1/4 Resolution – Quadrant and Dual VOUTa/VOUTc Modes



### Line Timing – Low Gain, High Gain and XLDR 1/4 Resolution – Single and Dual VOUTa/VOUTb Readout Modes

See Table 3 for device pin assignments

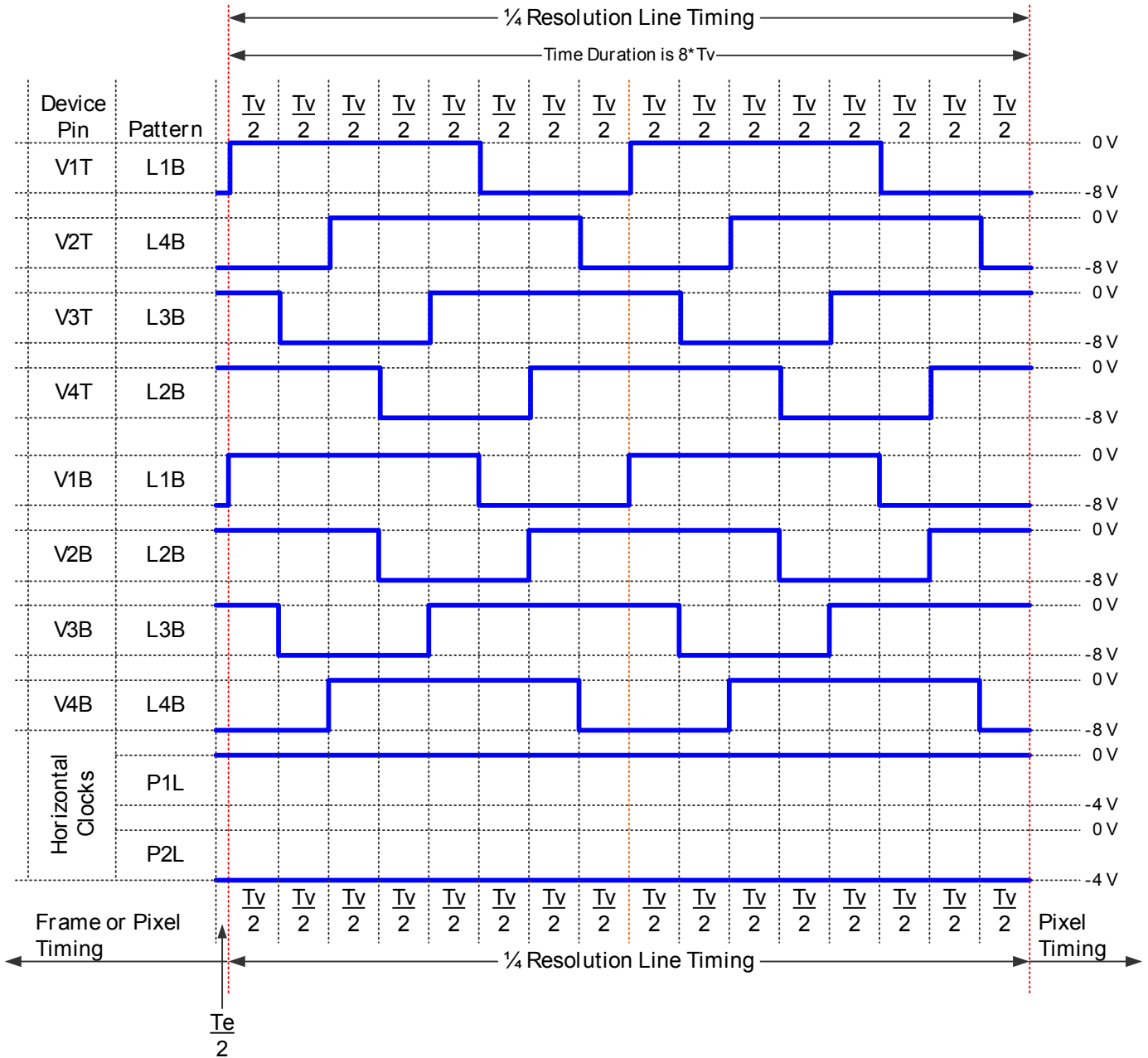


Figure 33: Line Timing Diagram – 1/4 Resolution – Single and Dual VOUTa/VOUTb Modes





### Electronic Shutter Timing Diagrams

The electronic shutter pulse can be inserted at the end of any line of the HCCD timing. The HCCD should be empty when the electronic shutter is pulsed. A recommended position for the electronic shutter is just after the last pixel is read out of a line. The VCCD clocks should not resume until at least  $T_v/2$  after the electronic shutter pulse has finished. The HCCD clocks can be run during the electronic shutter pulse as long as the HCCD does not contain valid image data.

For short exposures less than one line time, the electronic shutter pulse can appear inside the frame timing. Any electronic shutter pulse transition should be  $T_v/2$  away from any VCCD clock transition.

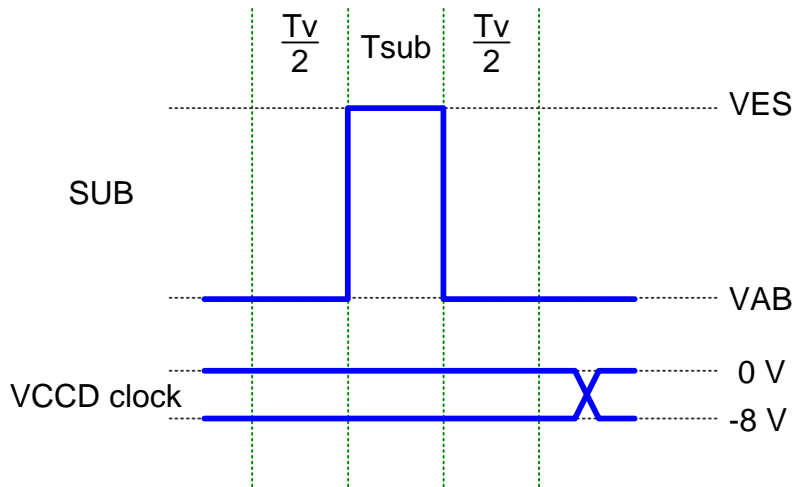


Figure 34: Electronic Shutter Timing

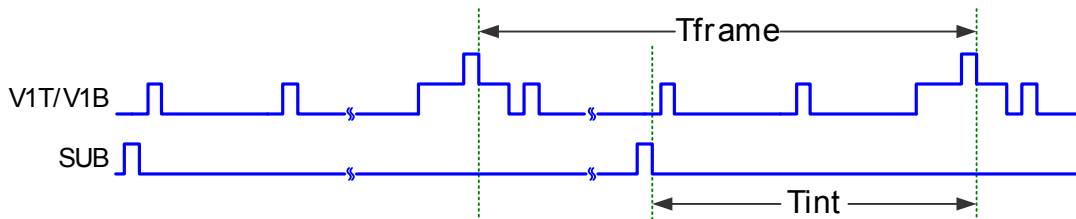


Figure 35: Frame/Electronic Shutter Timing



### Pixel Timing – Full Resolution – High Gain Pixel Timing

Use this timing to read out every pixel at high gain. If the sensor is to be permanently operated at high gain, the R2ab and R2cd pins can be left floating or set to any DC voltage between +3 V and +5 V. Note the R2ab and R2cd pins are internally biased to +4.3 V when left floating. The SHP1 and SHD1 pulses indicate where the camera electronics should sample the video waveform. The SHP1 and SHD1 pulses are not applied to the image sensor.

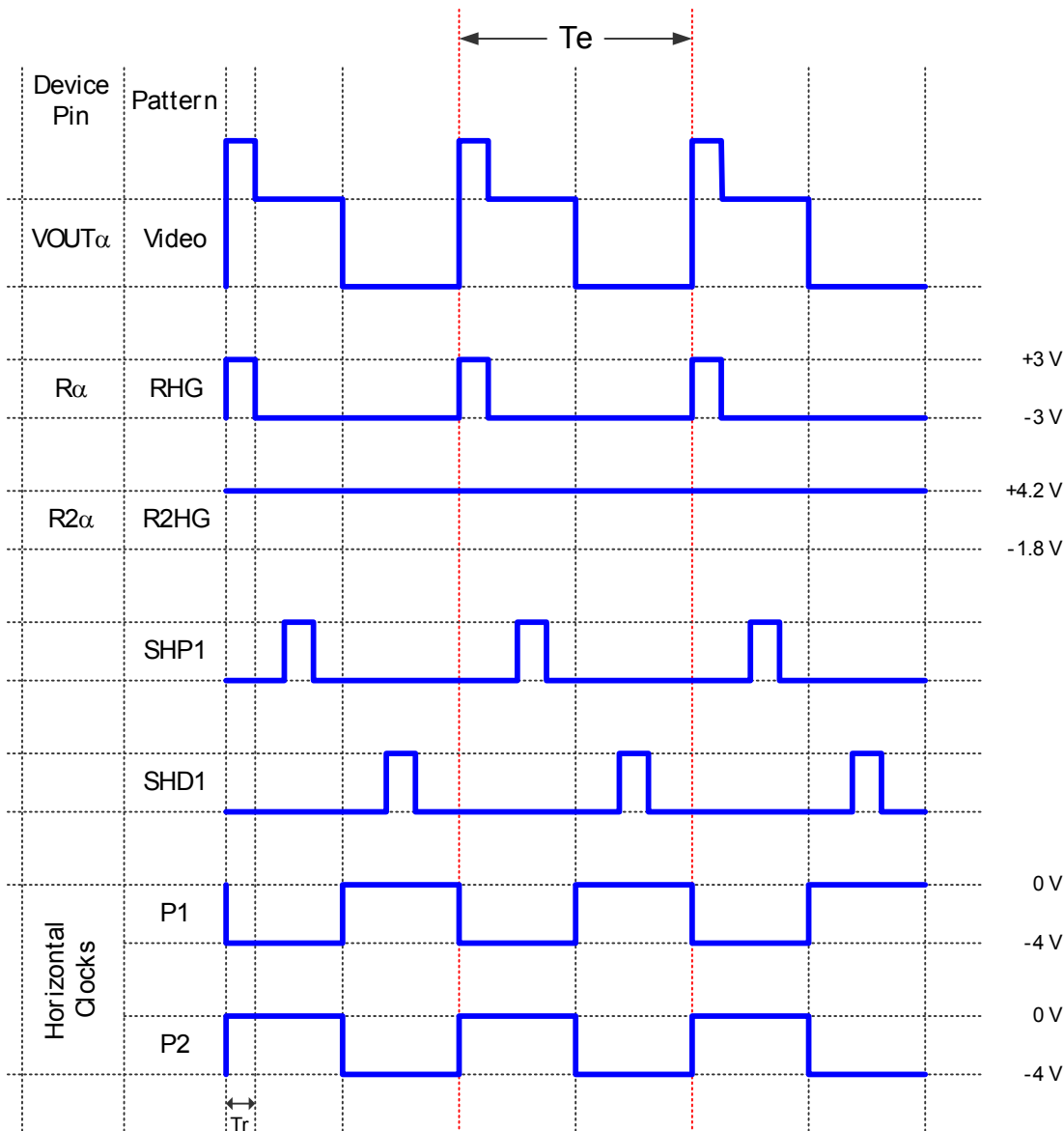


Figure 36: Pixel Timing Diagram – Full Resolution – High Gain



### Pixel Timing – Full Resolution – Low Gain Pixel Timing

Use this pixel timing to read out every pixel at low gain. If the sensor is to be permanently operated at low gain, the Ra, Rb, Rc and Rd pins should be set to any DC voltage between +3 and +5 V. The SHP1 and SHD1 pulses indicate where the camera electronics should sample the video waveform. The SHP1 and SHD1 pulses are not applied to the image sensor.

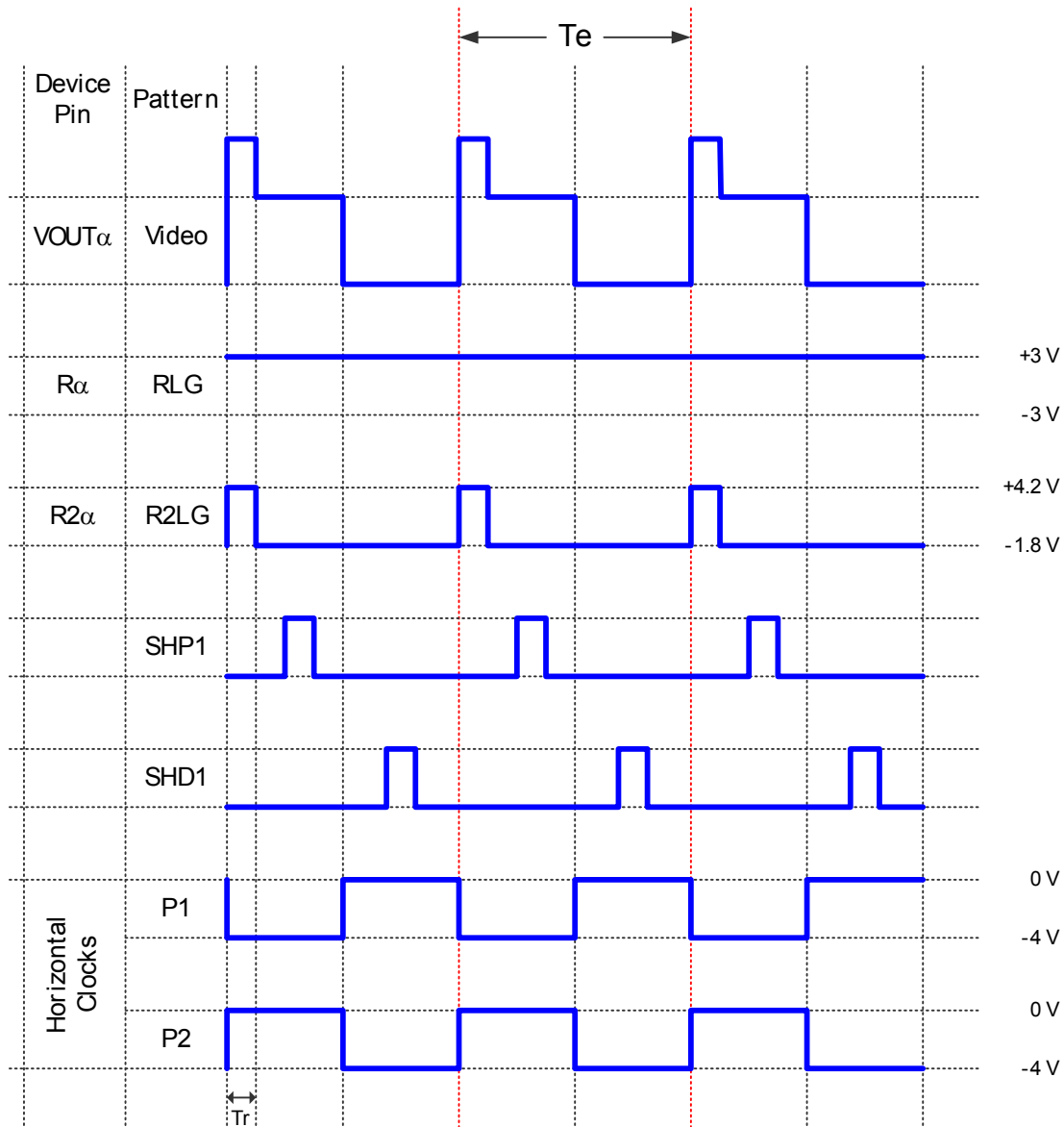


Figure 37: Pixel Timing Diagram – Full Resolution – Low Gain



### Pixel Timing – 1/4 Resolution – High Gain Pixel Timing

Use this timing to read out two pixels summed on the output amplifier sense node at high gain. If the sensor is to be permanently operated at high gain, the R2ab and R2cd pins can be left floating or set to any DC voltage between +3 V and +5 V. Note the R2ab and R2cd pins are internally biased to +4.3 V when left floating. The SHPQ and SHDQ pulses indicate where the camera electronics should sample the video waveform. The SHPQ and SHDQ pulses are not applied to the image sensor.

The Ra, Rb, Rc, and Rd pins are pulsed at half the frequency of the horizontal CCD clocks. This causes two pixels to be summed on the output amplifier sense node. The SHPQ and SHDQ clocks are also half the frequency of the horizontal CCD clocks.

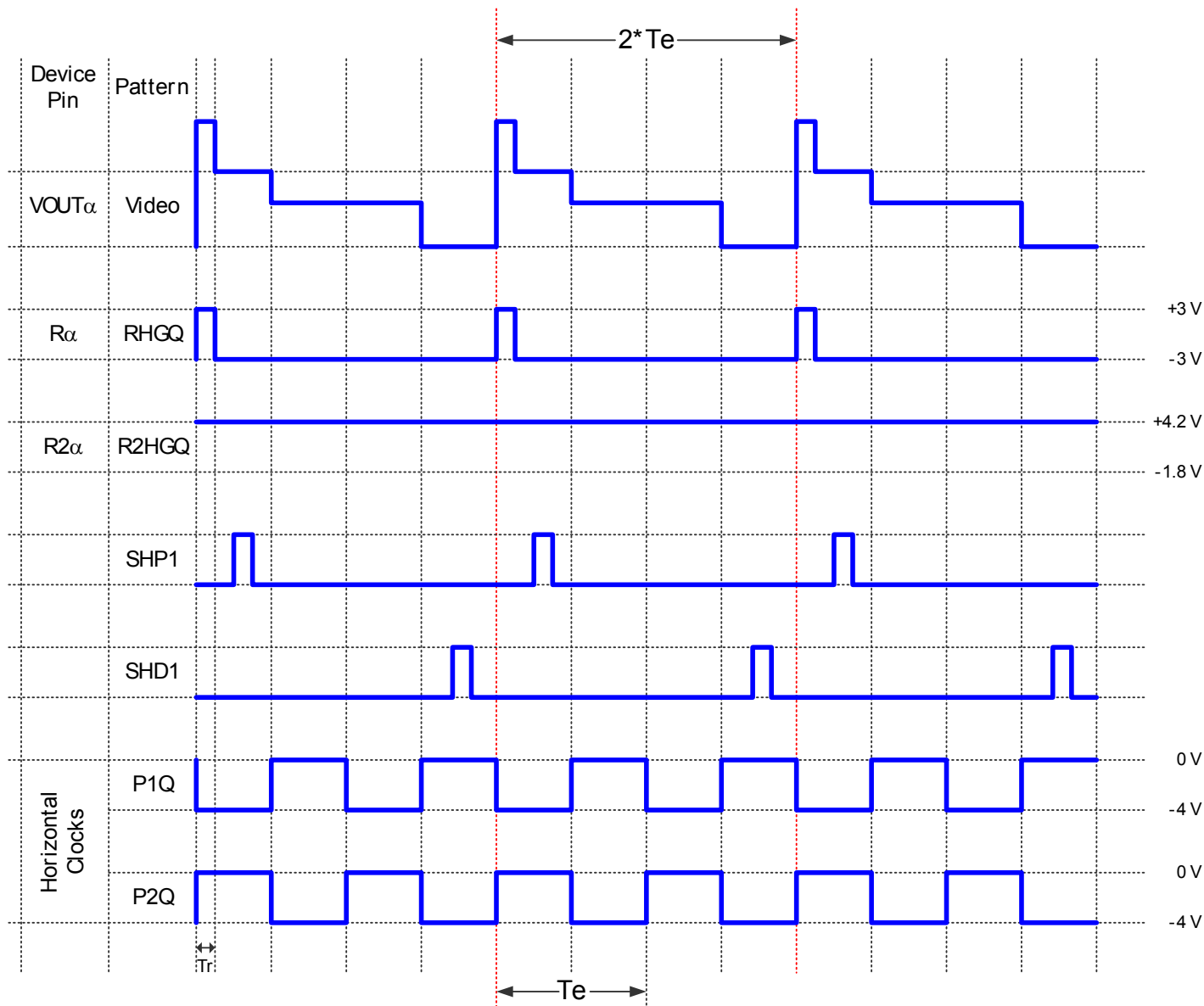


Figure 38: Pixel Timing Diagram – 1/4 Resolution – High Gain



### Pixel Timing – 1/4 Resolution – Low Gain Pixel Timing

Use this timing to read out two pixels summed on the output amplifier sense node at low gain. If the sensor is to be permanently operated at low gain, the Ra, Rb, Rc and Rd pins can be set to any DC voltage between +3 V and +5 V. The SHPQ and SHDQ pulses indicate where the camera electronics should sample the video waveform. The SHPQ and SHDQ pulses are not applied to the image sensor.

The R2ab and R2cd pins are pulsed at half the frequency of the horizontal CCD clocks. This causes two pixels to be summed on the output amplifier sense node. The SHPQ and SHDQ clocks are also half the frequency of the horizontal CCD clocks.

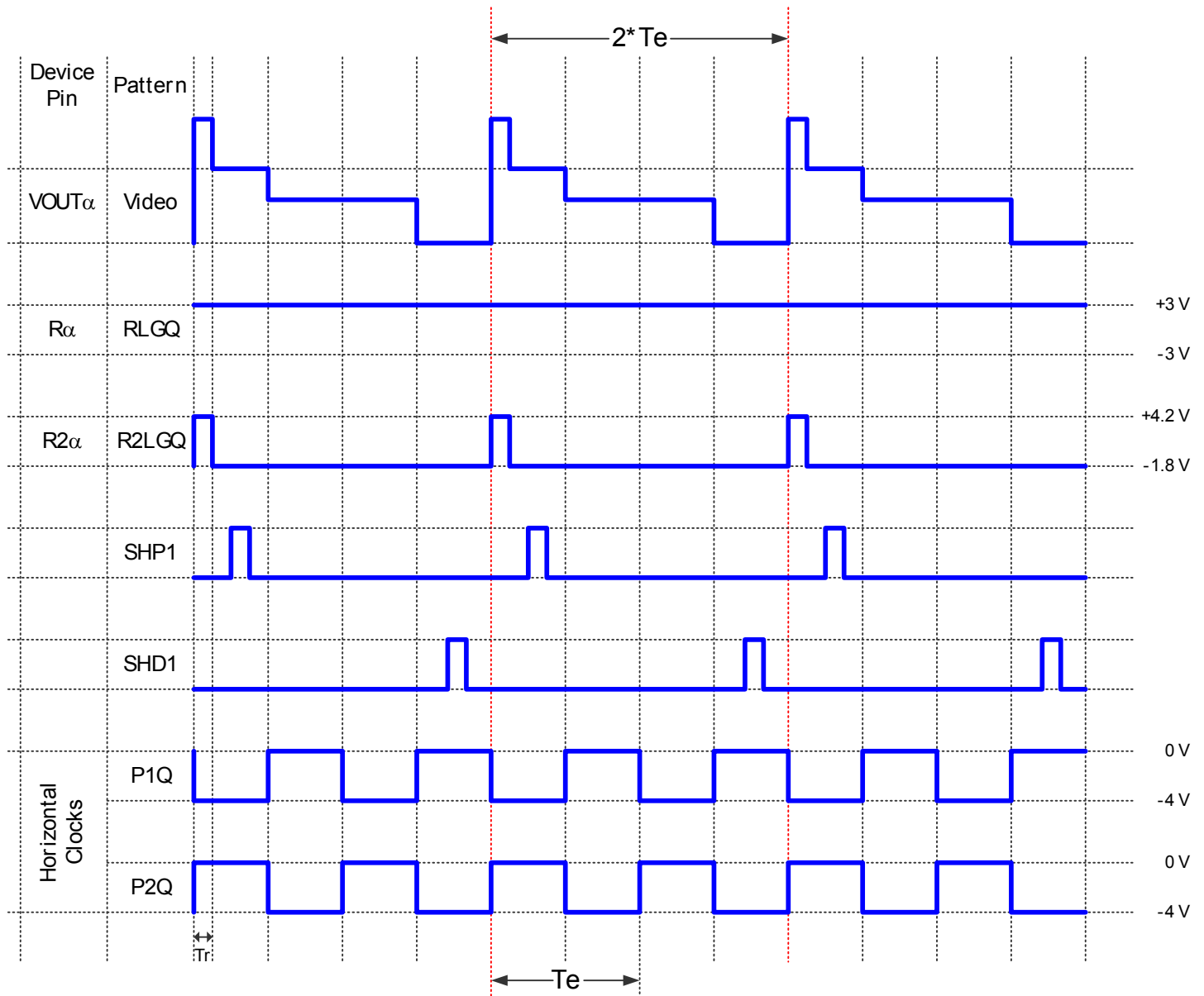


Figure 39: Pixel Timing Diagram – 1/4 Resolution – Low Gain



### XLDR Pixel Timing

To operate the sensor in extended linear dynamic range (XLDR) mode, the following pixel timing should be used. This mode requires two sets of analog front end (AFE) signal processing electronic units for each output. As shown in Figure 40 one AFE samples the pixel at low gain (SHPLG and SHDLG) and the other AFE samples the pixel at high gain (SHPHG and SHDHG).

Two HCCD pixels are summed on the output amplifier node to obtain enough charge to fully use the 82 dB range of the XLDR timing. Combined with two-line VCCD summing, a total of 160,000 electrons of signal (4x 40,000) can be sampled with 12 electrons or less noise. Note that a linear dynamic range of 82 dB is very large. Ensure that the camera optics is capable of focusing an 82 dB dynamic range image on the sensor. Lens flare caused by inexpensive optics or even dust on the lens will limit the dynamic range.

The timing shown in Figure 42 shows the HCCD not being clocked at a constant frequency. If the HCCD cannot be clocked at a variable frequency, then the HCCD may be clocked at a constant frequency (Figure 41) at the expense of about 33% slower frame rate.

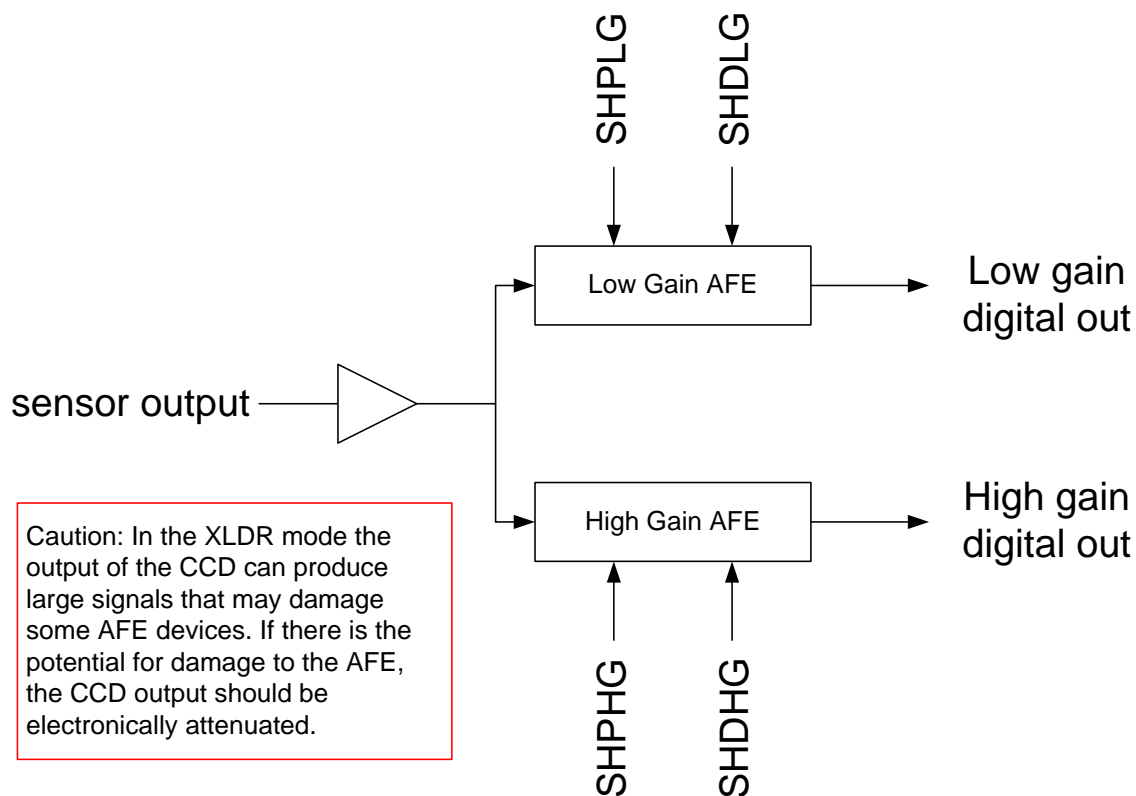


Figure 40: XLDR Timing - AFE Connections Block Diagram



**Pixel Timing – 1/4 Resolution – XLDR Pixel Timing – Constant HCCD Timing**

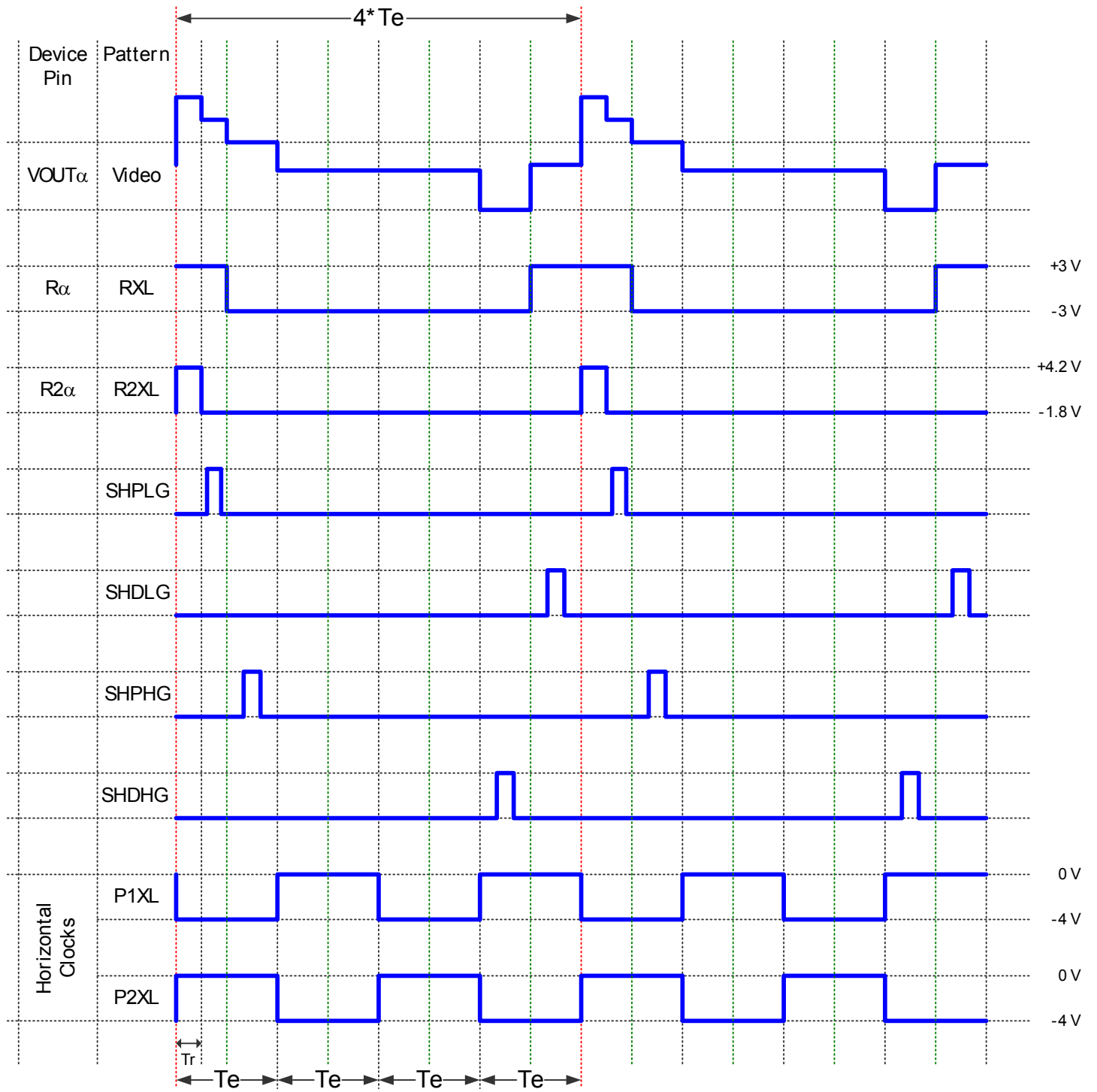


Figure 41: Pixel Timing Diagram – 1/4 Resolution – XLDR – Constant HCCD Timing



### Pixel Timing – 1/4 Resolution – XLDR Pixel Timing – Variable HCCD Timing

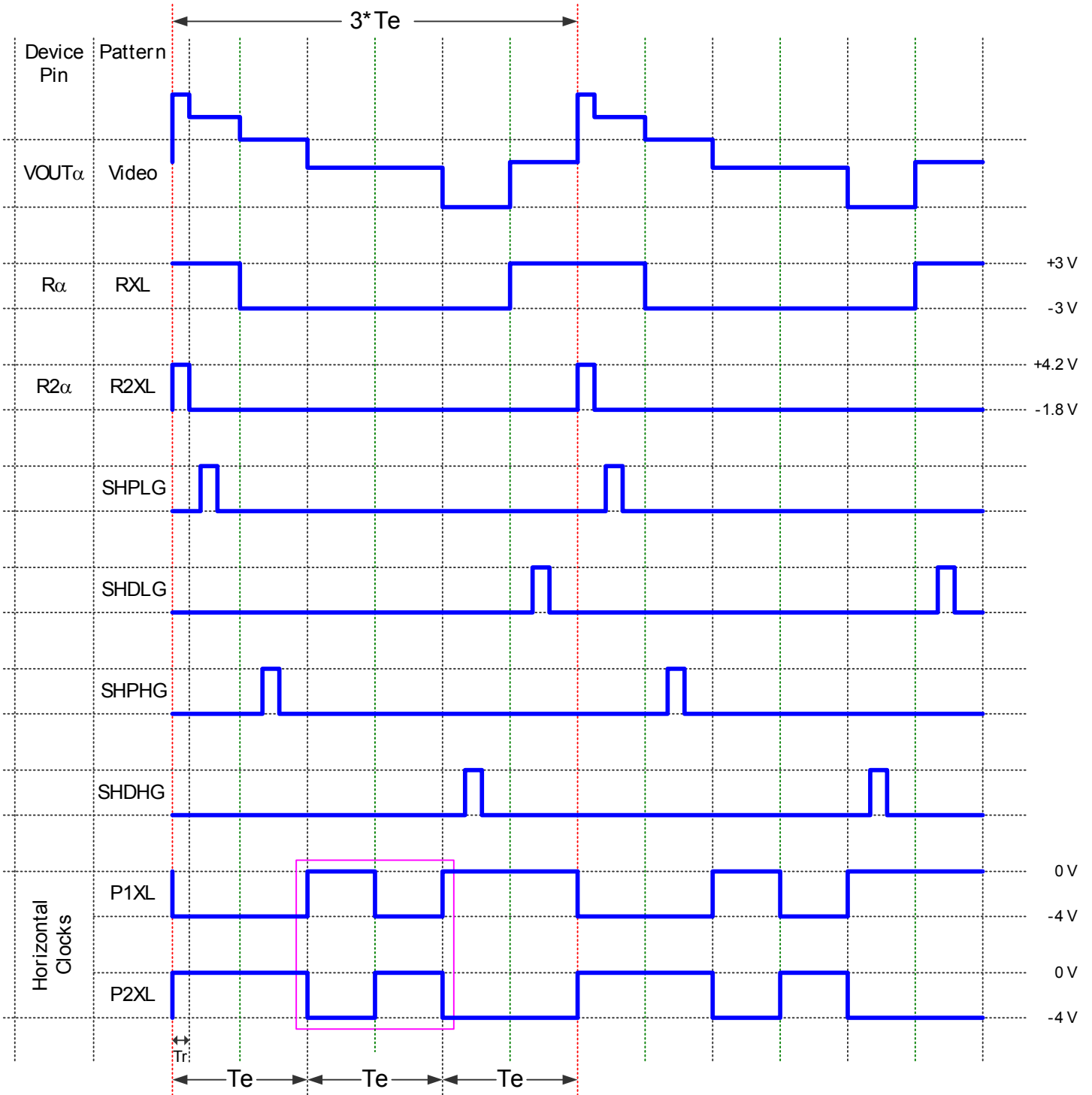


Figure 42: Pixel Timing Diagram – 1/4 Resolution – XLDR – Variable HCCD Timing





### VCCD Clock Edge Alignment

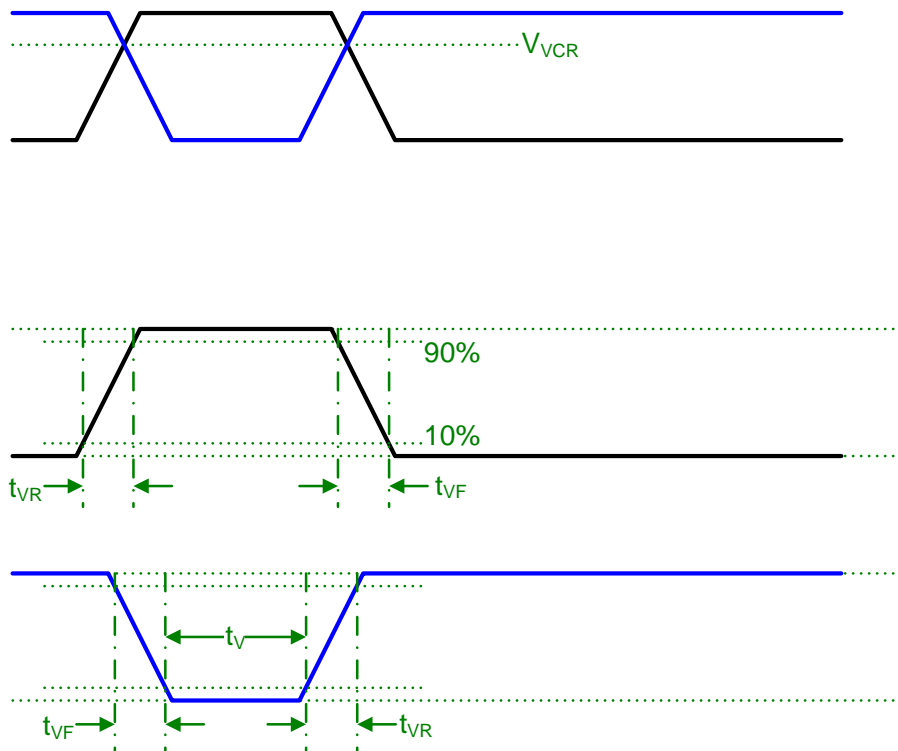


Figure 43: VCCD Clock Rise Time, Fall Time, and Edge Alignment



## Storage and Handling

### STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T <sub>ST</sub>	-55	+80	°C	1
Humidity	RH	5	90	%	2

#### Notes:

1. Long-term storage toward the maximum temperature will accelerate color filter degradation.
2. T=25 °C. Excessive humidity will degrade MTTF.

### ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

### COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

### ENVIRONMENTAL EXPOSURE

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

### SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.



## Mechanical Information

### COMPLETED ASSEMBLY

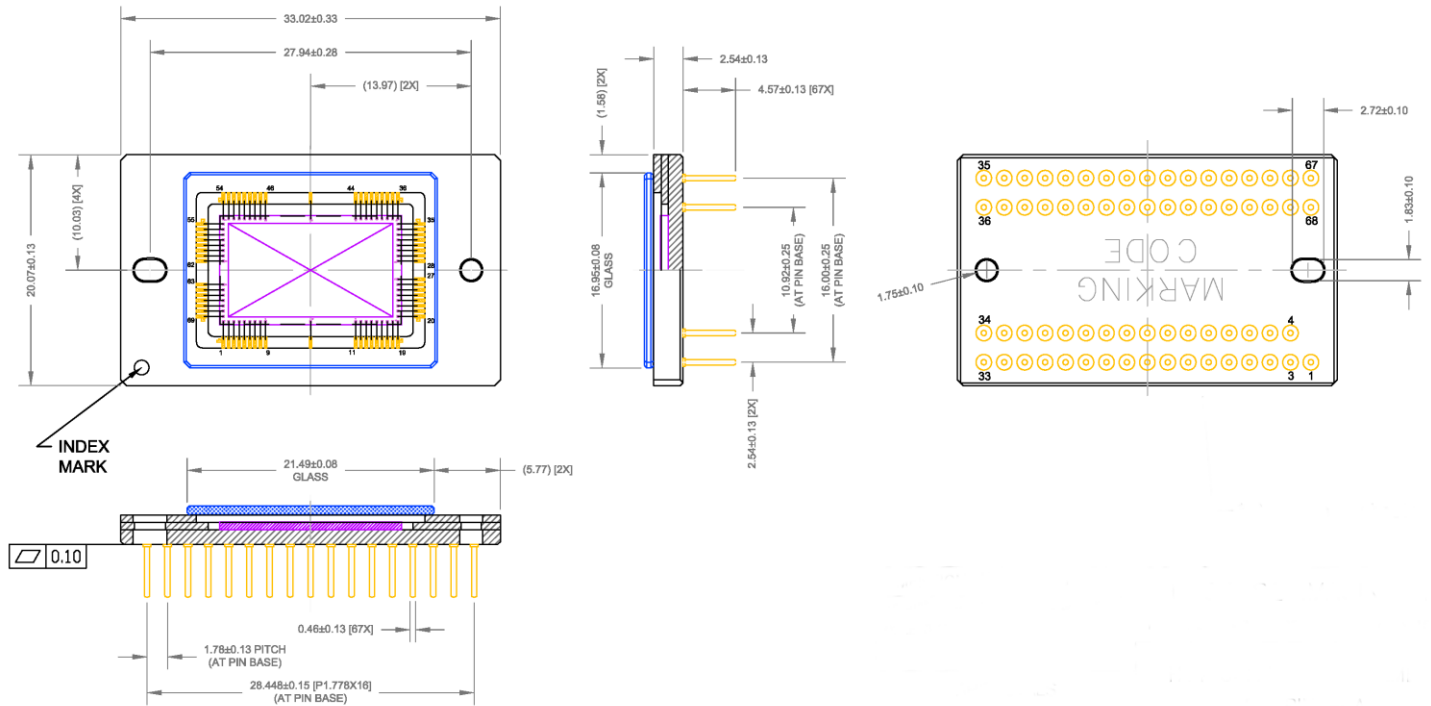


Figure 44: Completed Assembly (1 of 2)

Notes:

1. See Ordering Information for marking code.
2. No materials to interfere with clearance through package holes.
3. Units: mm

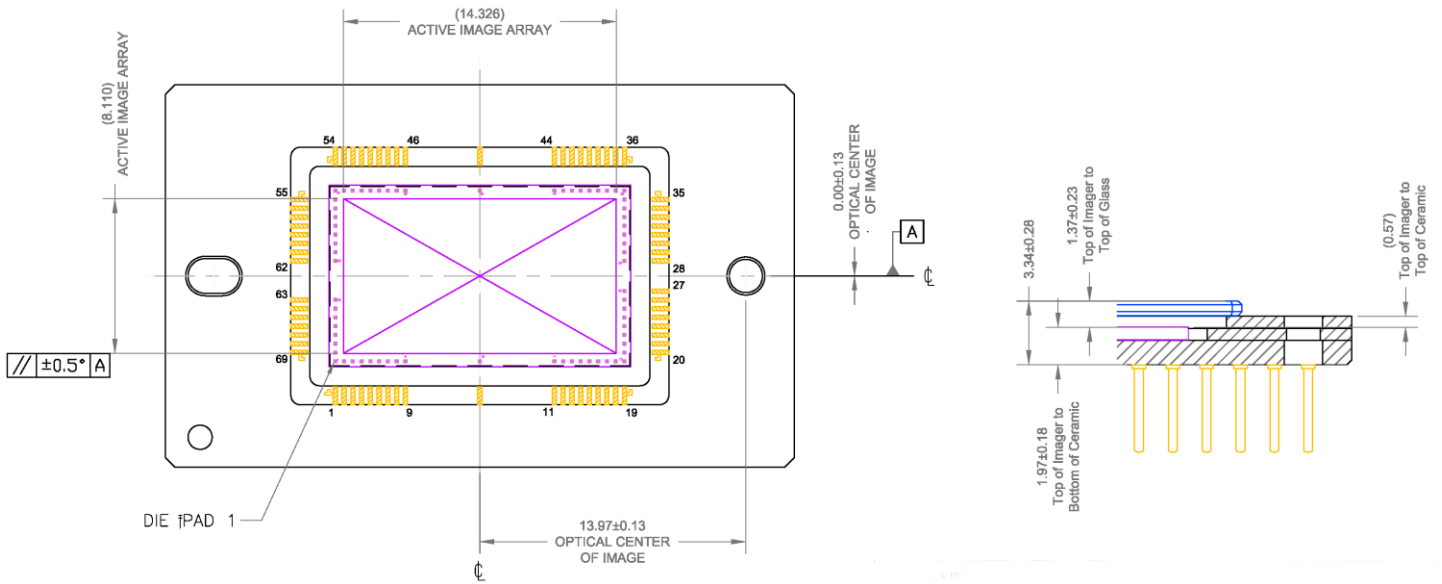


Figure 45: Completed Assembly (2 of 2)

Notes:

1. Optical center of image is nominally at the package center
2. Units: mm



COVER GLASS

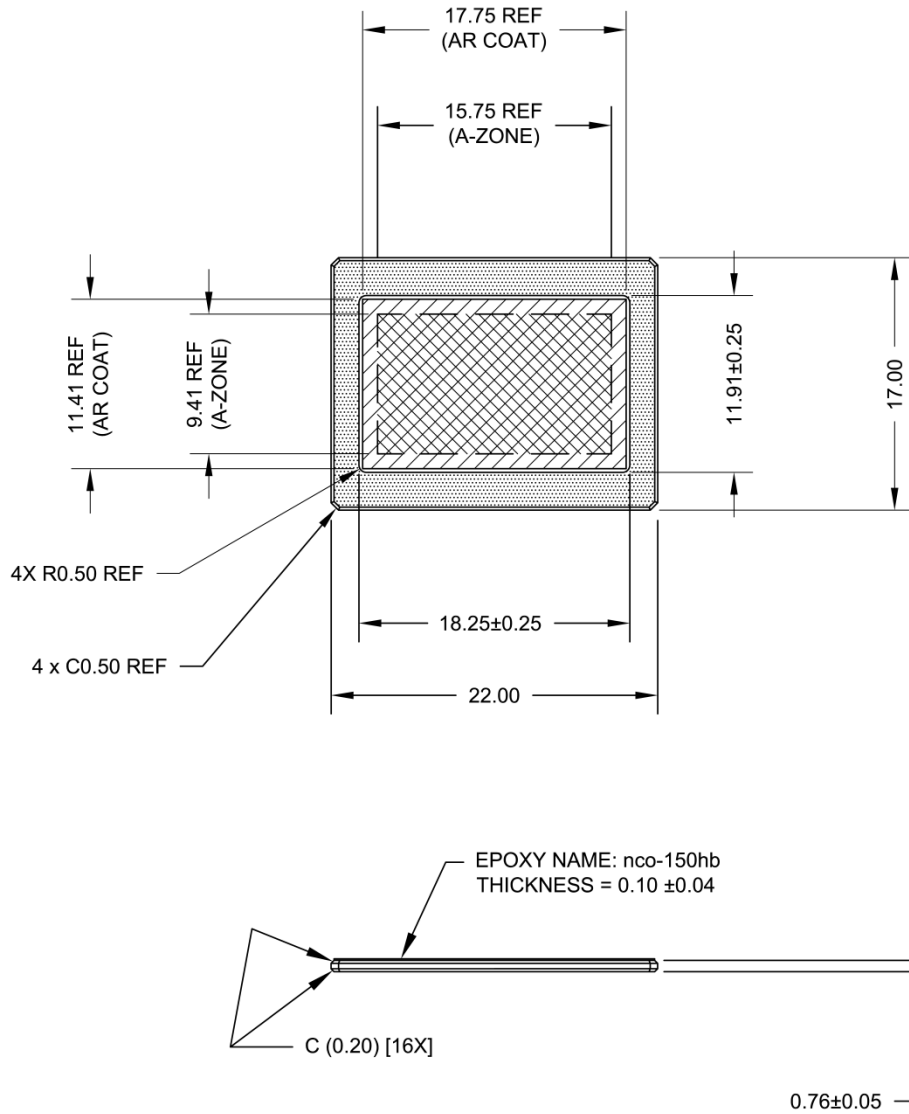


Figure 46: Cover Glass

Notes:

1. Substrate = Schott D263T eco
2. Dust, Scratch, Inclusion Specification: 10 μm maximum size in Zone A
3. MAR coated both sides
4. Spectral Transmission
  - a. T > 98.0% 420-435 nm
  - b. T > 99.2% 435-630 nm
  - c. T > 98.0% 630-680 nm
5. Units: mm



### COVER GLASS TRANSMISSION

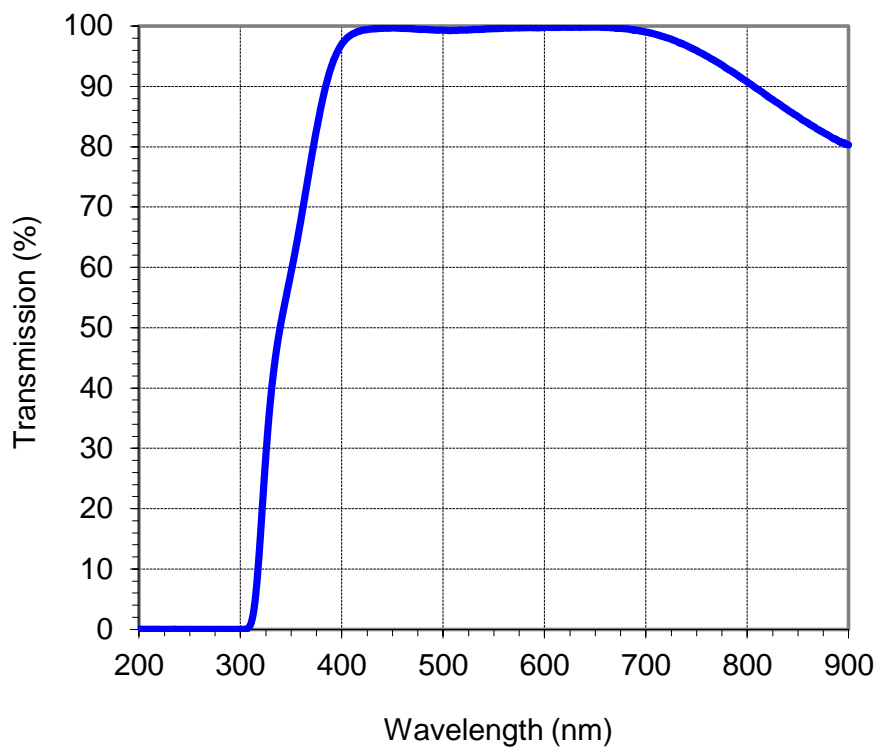


Figure 47: Cover Glass Transmission



## Quality Assurance and Reliability

### QUALITY AND RELIABILITY

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

### REPLACEMENT

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

### LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

### LIABILITY OF THE CUSTOMER

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

### TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

### MECHANICAL

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.


## Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.



## Revision Changes

Revision Number	Description of Changes
1.0	<ul style="list-style-type: none"> <li>Initial Release</li> </ul>
1.1	<ul style="list-style-type: none"> <li>Updated branding</li> </ul>

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**

Literature Distribution Center for ON Semiconductor  
 P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
 USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
 Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
 Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative